WEBINAR EMBARCADOS

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Segurança Funcional em Sistemas Embarcados:

IEC 61508, IEC 60730 e ISO 26262

Rogério Moreira

Gerente comercial / CEM - Customer Engagement Manager na Microchip

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Segurança Funcional em Sistemas Embarcados:

IEC 61508, IEC 60730 e ISO 26262

SMART | CONNECTED | SECURE

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Agenda

Introdução à Segurança Funcional

Processo de hardware

Processo de software

Normas técnicas

- IEC 61508
- IEC 60730
- ISO 26262

O que a Microchip oferece para suportar projetos com requisitos FuSa?

Produtos Microchip com suporte FuSa

- **AVR SD**

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Montadora faz ‘recall de 955 mil veículos no mundo por risco de software afetar câmera de ré

Montadora afirmou não ter conhecimento de acidentes ou feridos relacionados ao “recall”

Por David Shepardson, Em Reuters — Washington

17/08/2026 14h04 · Atualizado há 16 horas

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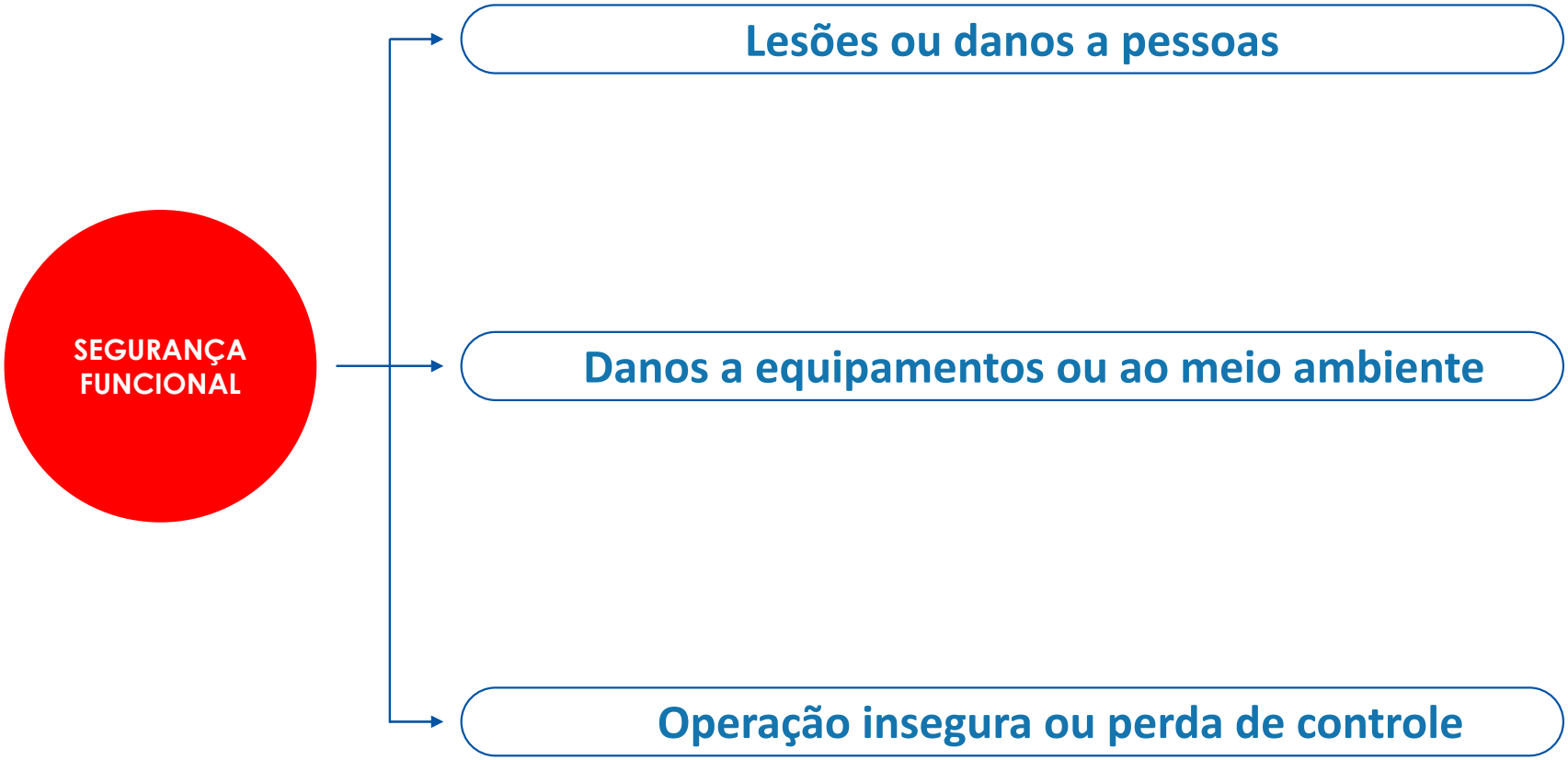
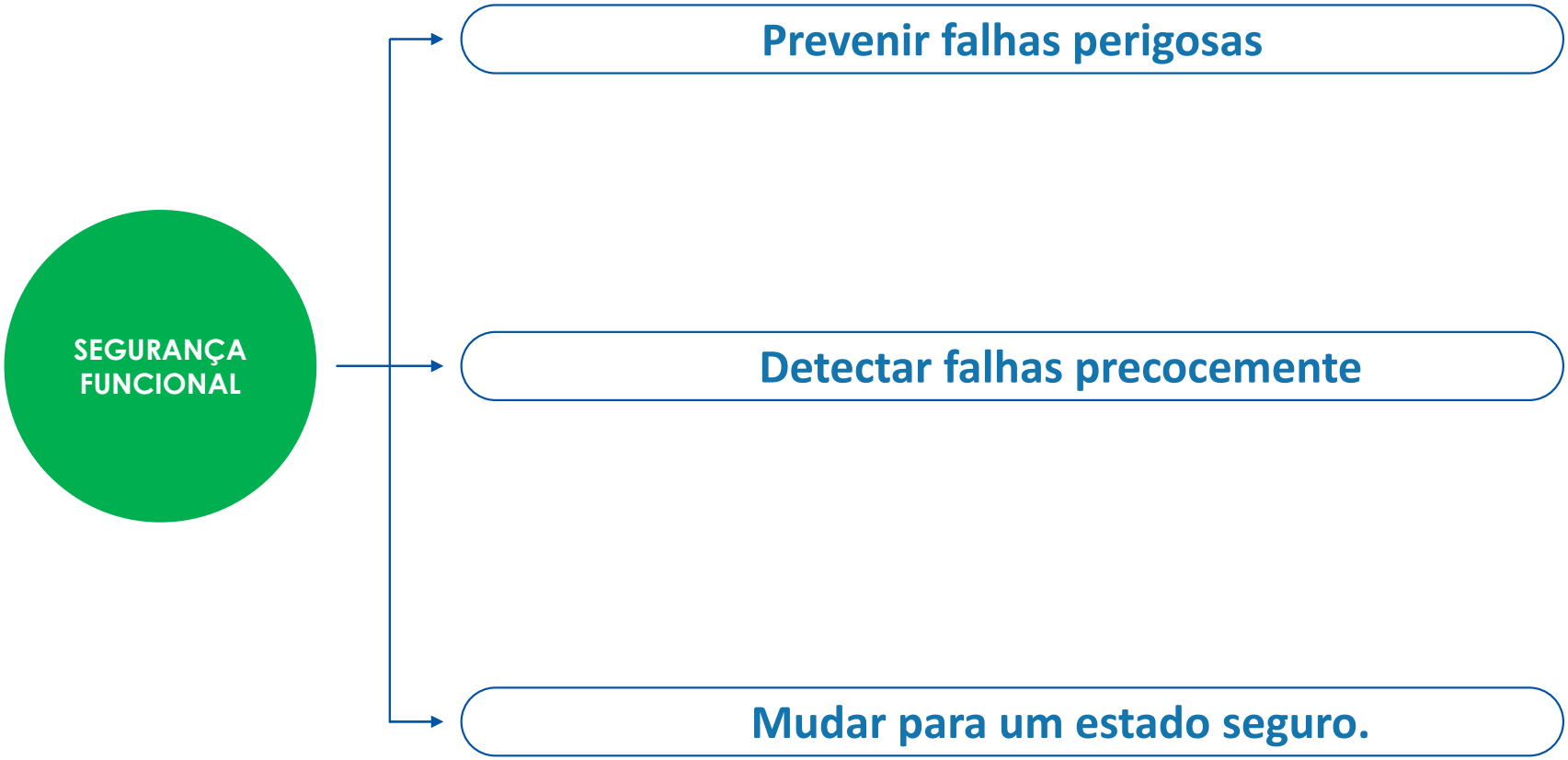
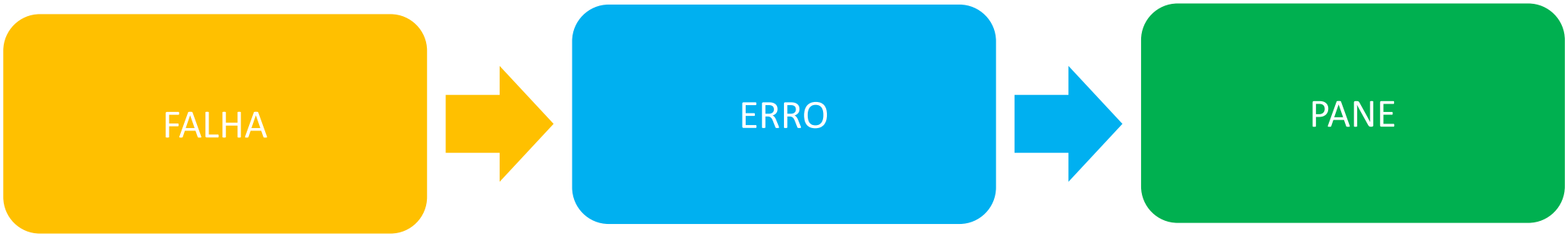

SEGURANÇA FUNCIONAL
Lesões ou danos a pessoas
Danos a equipamentos ou ao meio ambiente
Operação insegura ou perda de controle


SEGURANÇA FUNCIONAL
Prevenir falhas perigosas
Detectar falhas precocemente
Mudar para um estado seguro.



condição anormal
que pode levar
um elemento ou item
à falha

discrepância entre
um valor calculado ou medido
e o valor real

incapacidade de um elemento
de desempenhar uma função
conforme exigido

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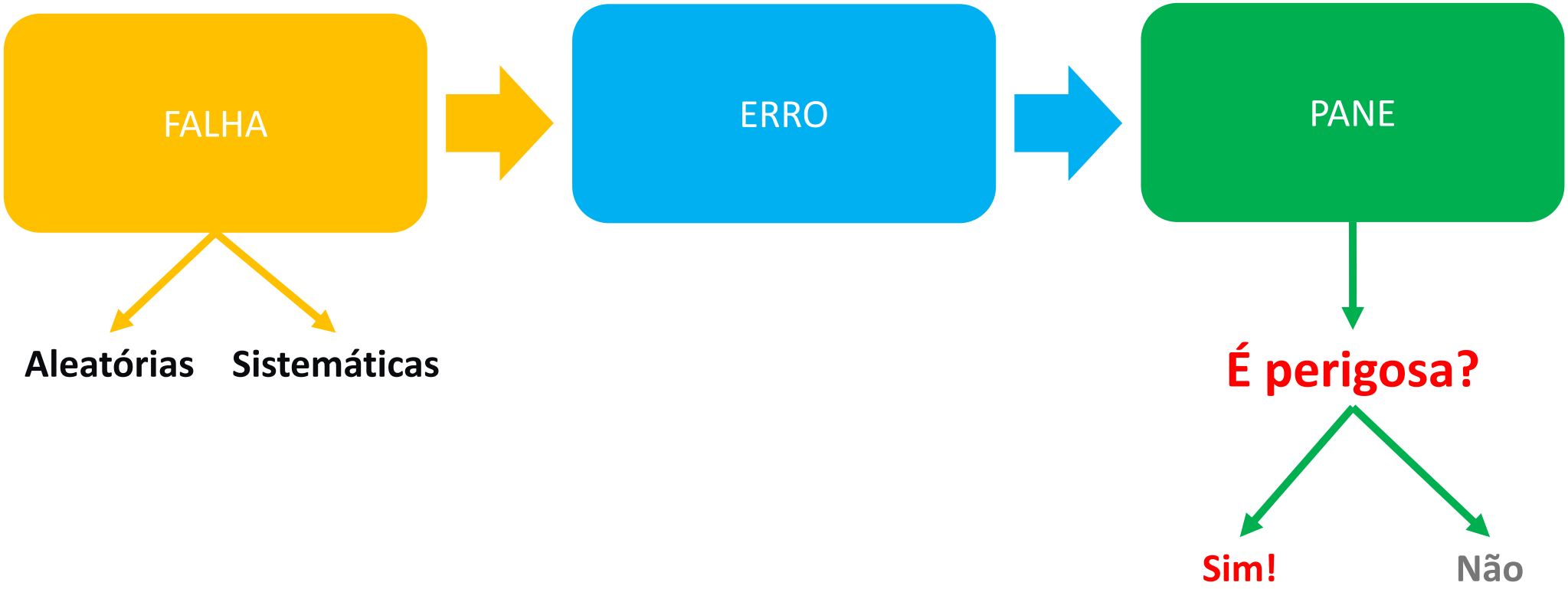

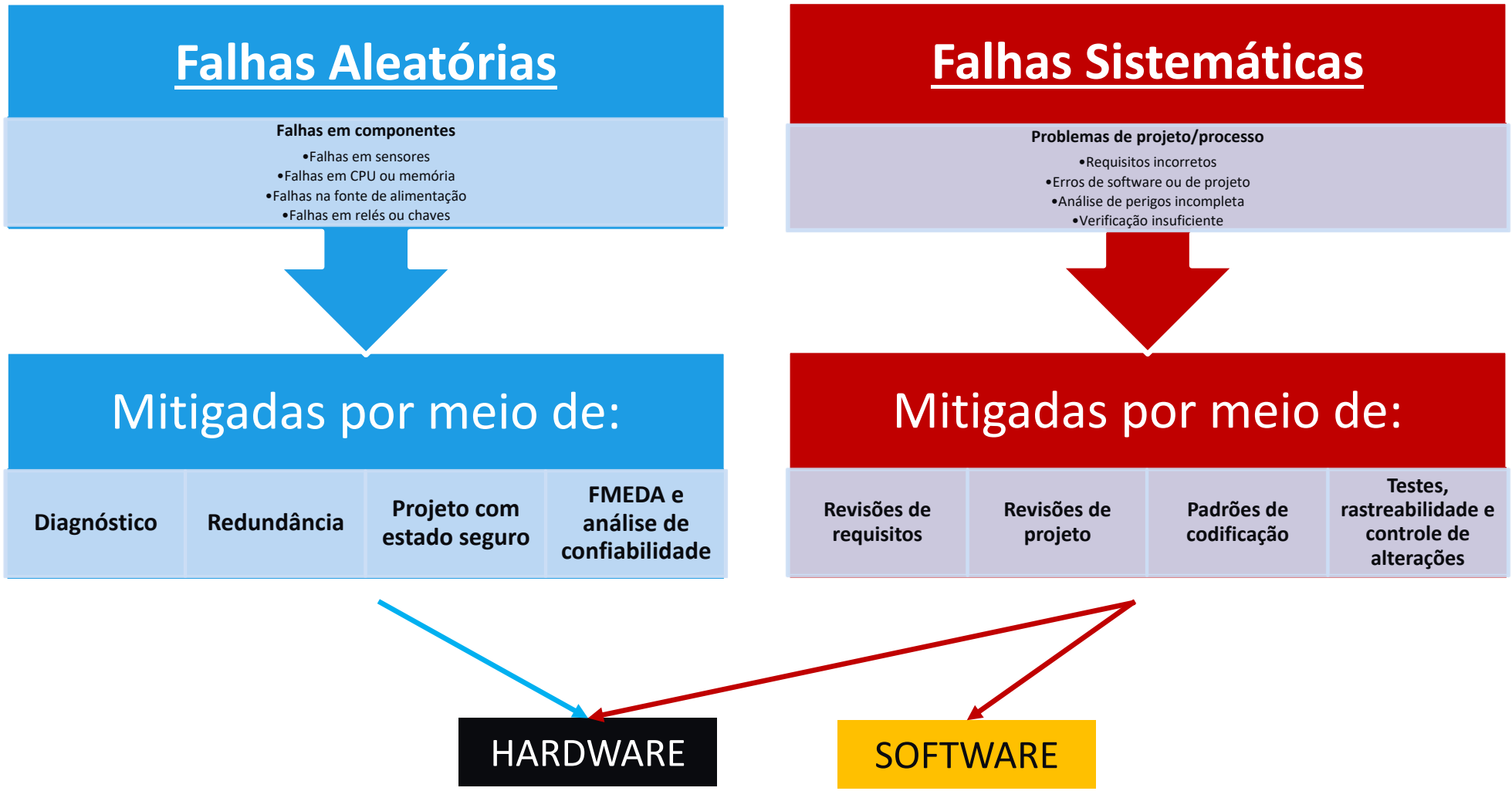

Processo de Hardware

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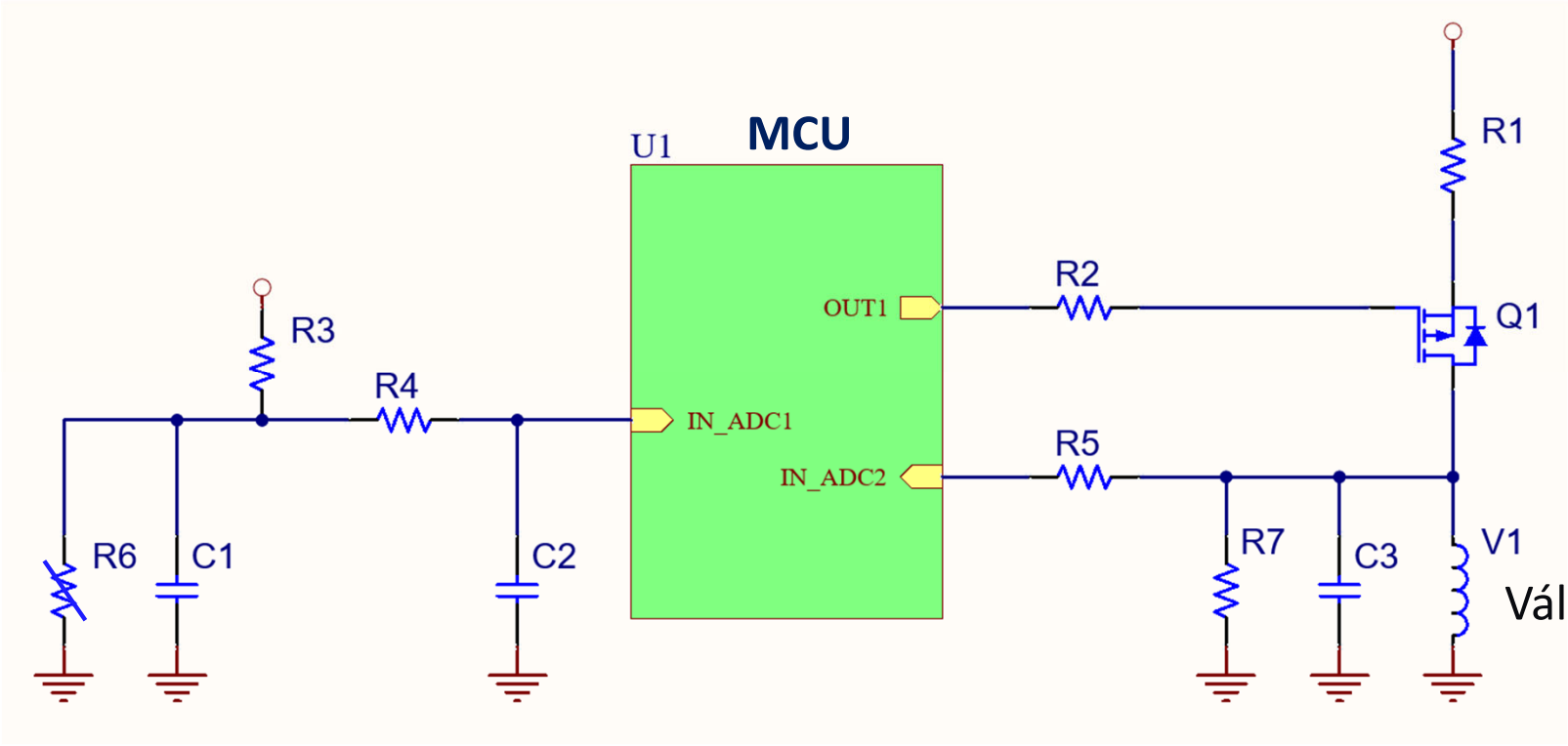
Análise de Hardware

- **Análise Dedutiva – *Top-Down***
  - Altamente recomendada –
    ASIL C, D
  - **Análise de Árvore de Falhas (FTA)**

- **Análise Indutiva – *Bottom-Up***
  - Altamente recomendada –
    ASIL A, B, C, D
  - **Análise de Modos de Falha, Efeitos e Diagnóstico (FMEDA)**

FTA – Análise dedutiva - Exemplo



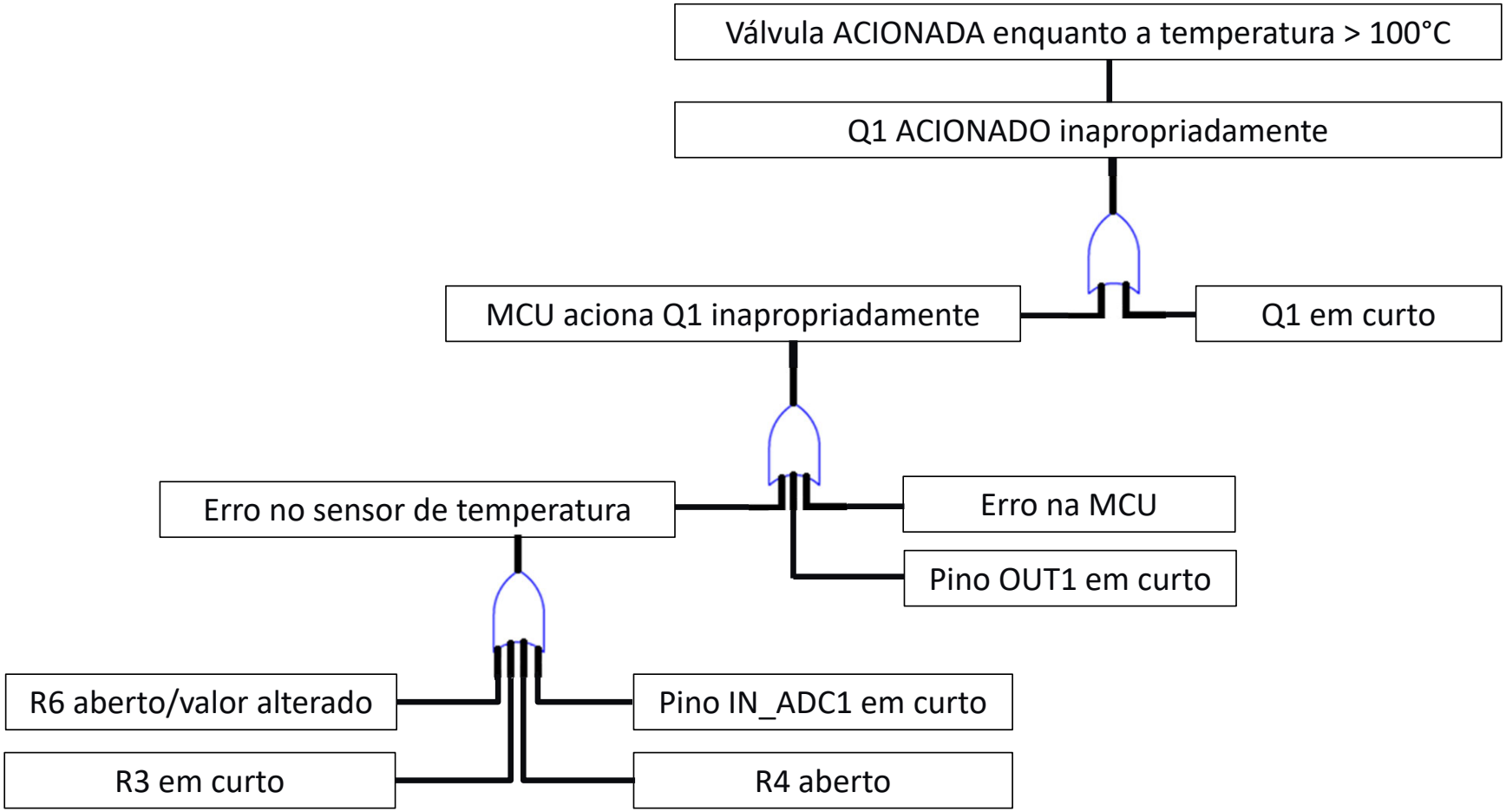
Termistor

Válvula

<u>Meta de segurança</u>:

A válvula V1 não deve ser alimentada por mais de 100 ms quando a temperatura estiver acima de 100°C.

FTA – Análise dedutiva - Exemplo



Arquiteturas de redundância

Arquitetura	Canais	Lógica de disparo	Segurança (PFD)	Disponibilidade (falso trip)	HFT
1oo1	1	o único canal decide	baixa	baixa robustez (sem redundância)	0
1oo2	2	qualquer 1 dos 2 dispara	alta	menor (mais suscetível a trip espúrio)	1
2oo2	2	os 2 precisam concordar	menor	alta	0
2oo3	3	2 dos 3 concordam	alta	alta	1

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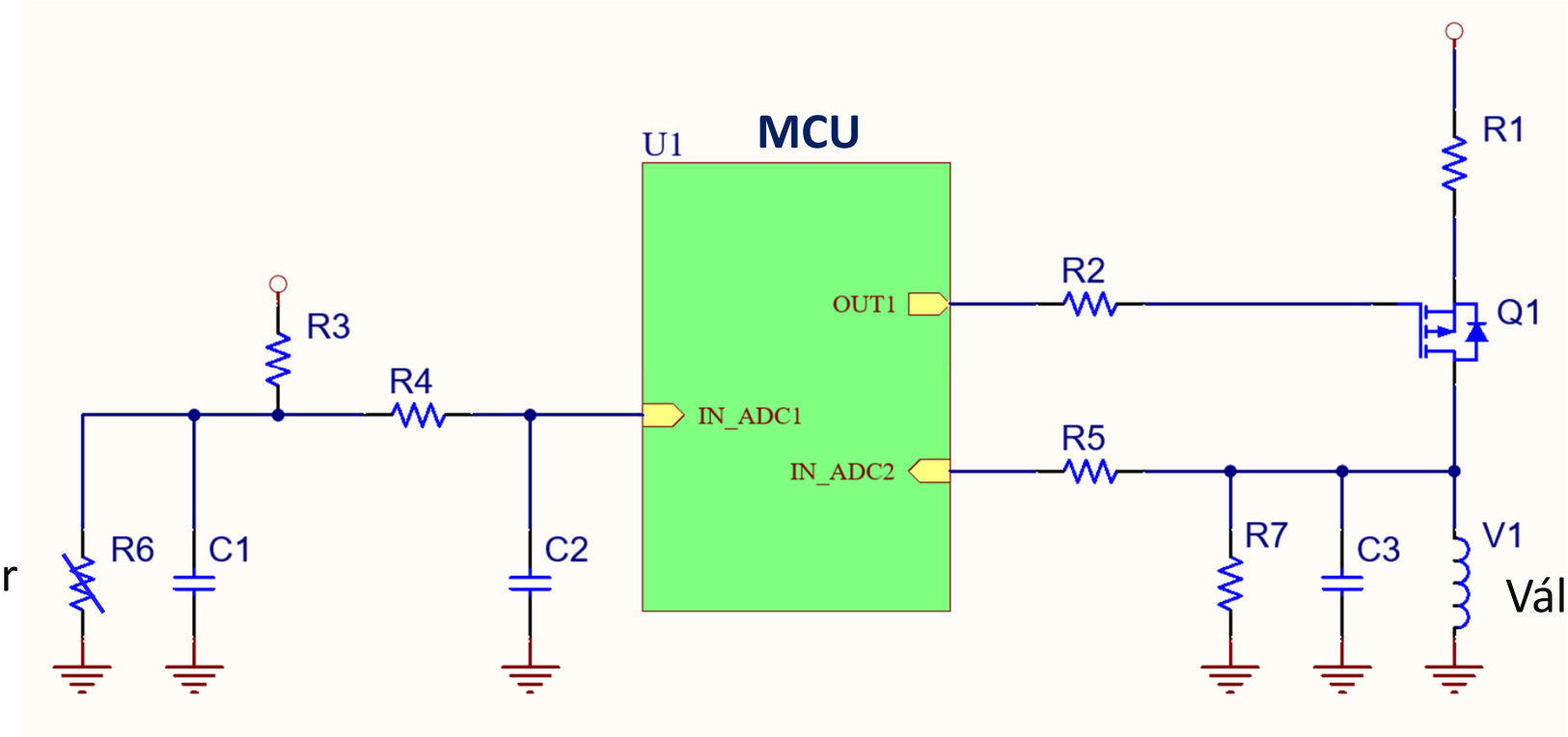
FMEDA – Análise indutiva - Exemplo



Termistor

Válvula

<u>Meta de segurança</u>:

A válvula V1 não deve ser alimentada por mais de 100 ms quando a temperatura estiver acima de 100°C.

FMEDA do sistema

Component	FIT	Safety Related?	Failure Mode	Distribution	Potential to Violate SG?	Safety Mechanism	Failure Mode Coverage	Residual or Single-Point FIT	Can Violate SG with Another Fault?	Safety Mechanism	Failure Mode Coverage (Latent)	Latent MPF FIT
R1	2	no	open	90%	no							
			short	10%	no							
R2	2	yes	open	90%	yes	none	0%	1.8				
			short	10%	no							
Q1	5	yes	open	50%	no							
			short	50%	yes	SM1	90%	0.25	yes	SM1	80%	0.45
V1	5	no	open	80%	no							
			short	20%	no							
C3	2	no	open	20%	no							
			short	80%	no							
R7	2	no	open	90%	no							
			short	10%	no							

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FMEDA do sistema

Component	FIT	Safety Related?	Failure Mode	Distribution	Potential to Violate SG?	Safety Mechanism	Failure Mode Coverage	Residual or Single-Point FIT	Can Violate SG with Another Fault?	Safety Mechanism	Failure Mode Coverage (Latent)	Latent MPF FIT
R5	2	yes	open	90%	no				yes	none	0%	1.8
			short	10%	no							
U1	100	yes	all	50%	yes	WDT	90%	5				
			all	50%	no							
	131						**Total**	**10.85**			**Total**	**2.25**

Total failure rate: 131 FIT
Total non-safety: 15 FIT
Total safety-related: 116 FIT

Single-point fault: 10.85 FIT
Latent fault: 2.25 FIT

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Processo de Firmware

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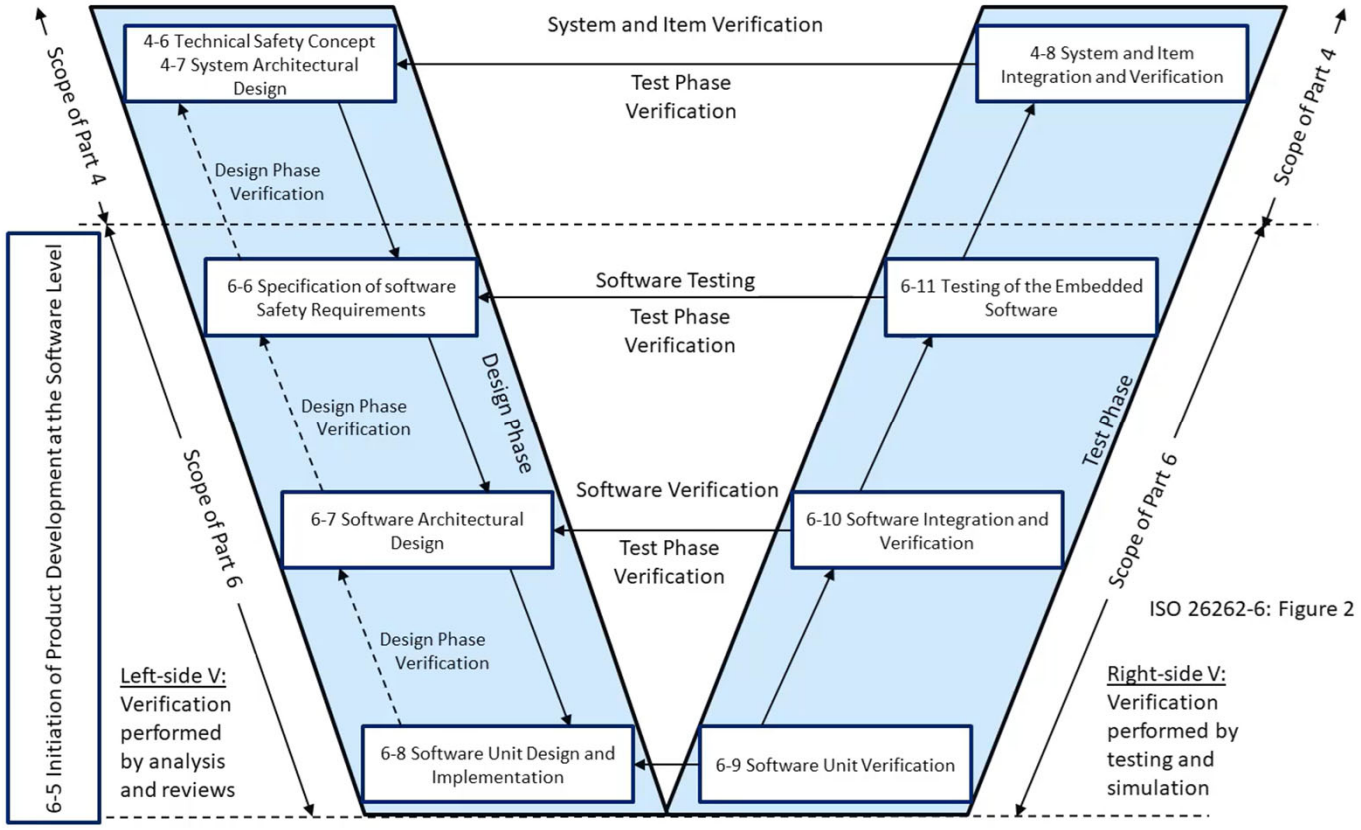
Ciclo de vida de projeto com FuSa



ISO 26262-6: Figure 2

Desenvolvimento do FIRMWARE

- Rastreabilidade de requisitos
- Padrões de codificação
- **Análise estática**
- Revisão por pares
- Testes unitários
- Testes de integração
- Qualificação de ferramentas
- Gerenciamento de configuração
- Controle de alterações

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Static Analysis

Perforce Static Analysis

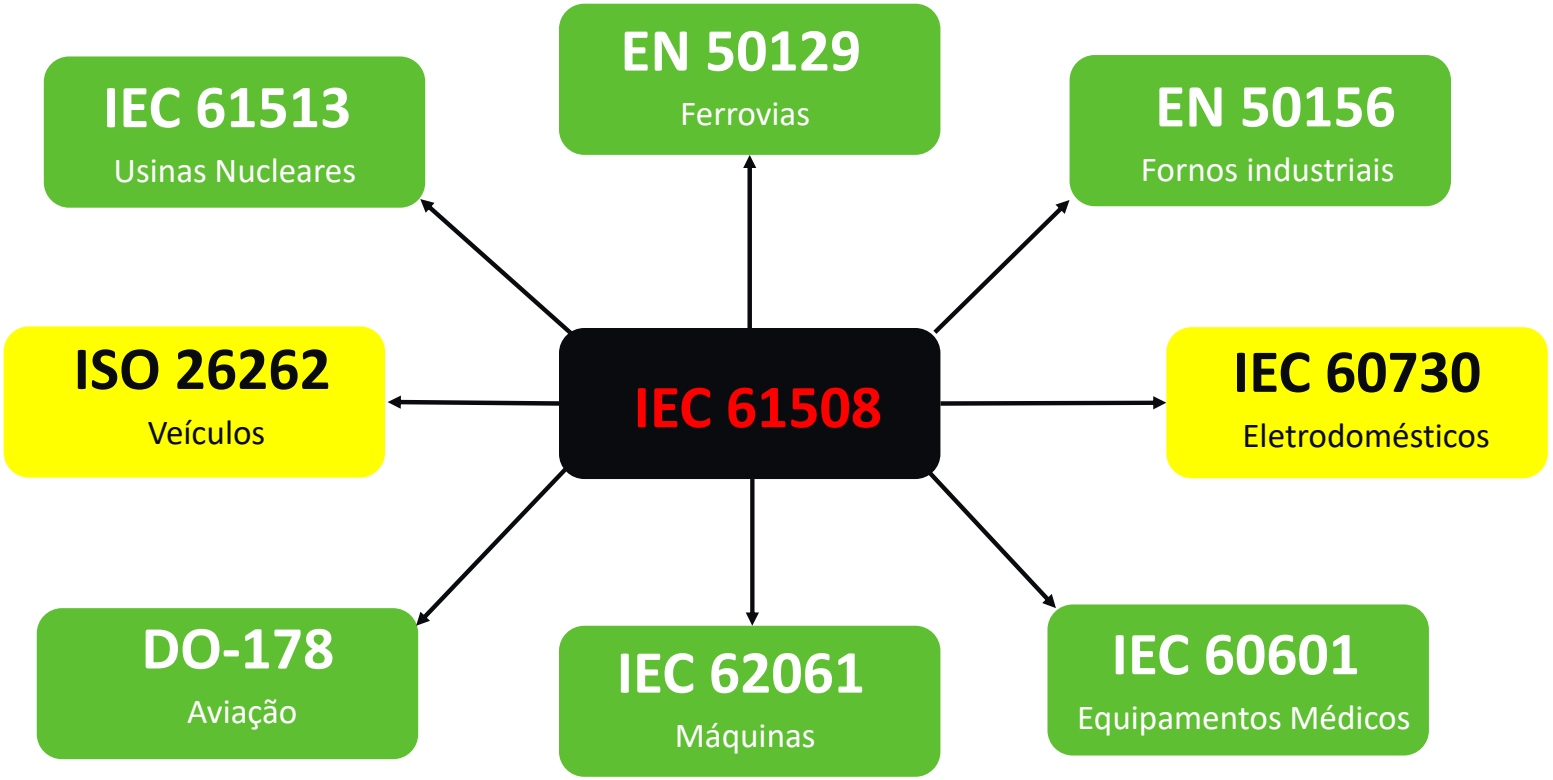
For Safe, Secure, High-Quality Code. Faster.

Static analysis identifies defects, vulnerabilities, and compliance issues as you code. It finds issues that are often missed by other tools and methods, such as compilers and manual code reviews. With static analysis, you can fix coding issues earlier — lowering overall costs and enabling you to deliver a quality product on time.

- Improve Software Quality
- Comply with Coding Standards
- Code with Confidence
- Reduce Technical Debt

https://www.perforce.com/

Normas técnicas



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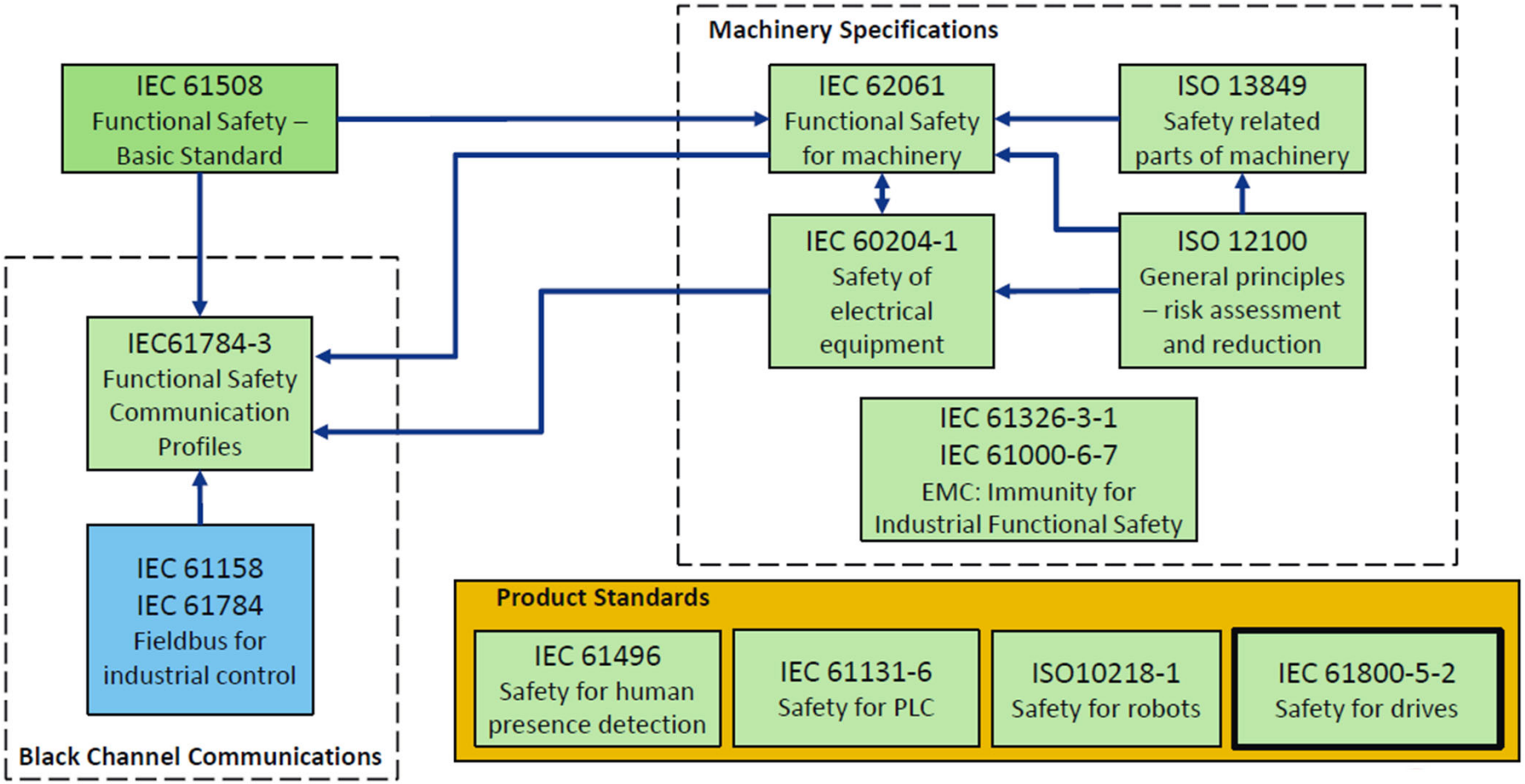
FuSa Specifications for Industrial Automation



IEC 61508

IEC 61508 – a norma “mãe” da Segurança Funcional

Part	Title	Status	Scope Summary	Pages	Cost (CHF)
IEC 61508-1	General requirements	Normative	Defines the overall safety lifecycle, functional safety management, and the framework for Safety Integrity Levels (SILs). It contains the master requirements that govern all other parts.	127	$380
IEC 61508-2	Requirements for E/E/PE safety-related systems	Normative	Specifies the requirements for designing and managing safety-related hardware, including architectural constraints and probabilistic analysis to control random hardware failures.	187	$405
IEC 61508-3	Software requirements	Normative	Details the requirements for the software safety lifecycle, from specification through design, coding, and testing, to control systematic failures in software.	234	$405
IEC 61508-4	Definitions and abbreviations	Normative	Provides the official definitions for terms and abbreviations used throughout the standard, ensuring a common vocabulary.	68	$260
IEC 61508-5	Examples of methods for the determination of safety integrity levels	Informative	Offers guidance and examples of different methodologies (e.g., risk graphs, LOPA) that can be used to determine the required SIL for a safety function.	97	$295
IEC 61508-6	Guidelines on the application of IEC 61508-2 and IEC 61508-3	Informative	Provides practical guidance, particularly on quantitative analysis and the application of the hardware and software requirements from Parts 2 and 3.	237	$405
IEC 61508-7	Overview of techniques and measures	Informative	Describes a wide range of techniques and measures referenced in Parts 2 and 3, explaining their purpose and providing guidance on their application for fault control and avoidance.	296	$430
				1246	$2,580

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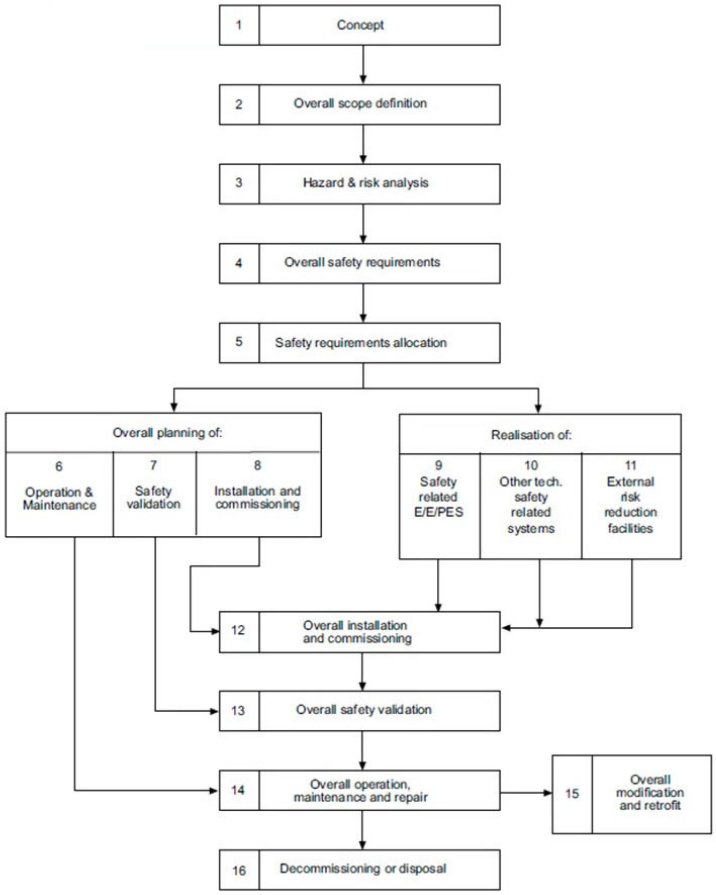
IEC 61508 – CICLO DE VIDA

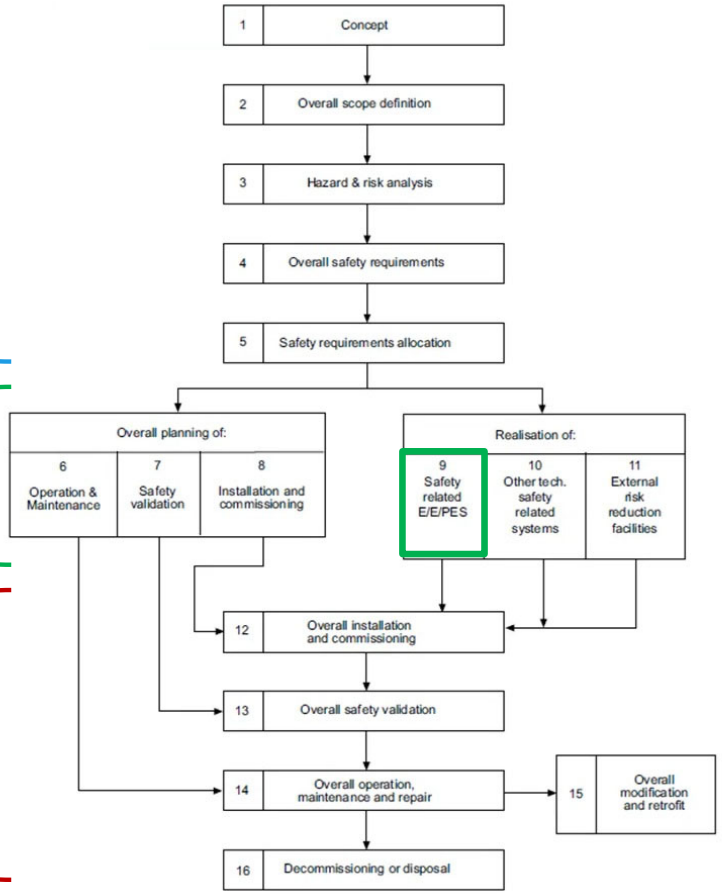


IEC 61508 – CICLO DE VIDA

Análise

Realização

Operação e modificação



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SIL
Safety Integrity Level

- Métrica de desempenho que indica o **grau de redução de risco** oferecido por um sistema de Segurança Funcional.
- Ele quantifica a **probabilidade de um sistema falhar** em executar sua função de proteção.

Nível SIL	Modo de Baixa Demanda (PFDavg)	Modo de Alta Demanda ou Contínuo (PFH por hora)	Fator de Redução de Risco (RRF)
SIL 1	>= 10^{-2} a < 10^{-1}	>= 10^{-6} a < 10^{-5}	10 a 10^{2}
SIL 2	>= 10^{-3} a < 10^{-2}	>= 10^{-7} a < 10^{-6}	10^{2} a 10^{3}
SIL 3	>= 10^{-4} a < 10^{-3}	>= 10^{-8} a < 10^{-7}	10^{3} a 10^{4}
SIL 4	>= 10^{-5} a < 10^{-4}	>= 10^{-9} a < 10^{-8}	10^{4} a 10^{5}

Baixo risco

Alto risco

Métodos de Determinação:

- **HAZOP**
- **LOPA**
- **FMEA**
- **FMEDA**
- **FTA**

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SIL – Safety Integrity Level

Matriz de risco

		Probabilidade				
		Frequente	Provável	Ocasional	Rara	Improvável
Severidade		**E**	**D**	**C**	**B**	**A**
Catastrófica	**IV**	Inaceitável	Inaceitável	SIL 4	SIL 3	SIL 2
Crítica	**III**	Inaceitável	SIL 4	SIL 3	SIL 2	SIL 1
Marginal	**III**	SIL 3	SIL 3	SIL 2	SIL 1	Risco aceitável
Insignificante	**I**	SIL 2	SIL 1	Risco aceitável	Risco aceitável	Risco aceitável

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FUNCTIONAL SAFETY — IEC 61508

Como determinar o SIL de um sistema elétrico/eletrônico

Duas fases: a análise de risco define o SIL necessário; o projeto e sua verificação comprovam o SIL alcançado.

SIL NECESSÁRIO · análise de risco

1 — Definir a função de segurança

Escopo, evento perigoso e fronteiras do sistema (sensor → lógica → atuador).

2 — Analisar perigos e riscos

HAZOP, "what-if" ou FMEA de processo para identificar causas e eventos.

3 — Avaliar o risco sem proteção

Severidade, frequência da causa e exposição, sem a camada em análise.

4 — Aplicar método de SIL e obter o RRF

LOPA, risk graph ou matriz de risco → fator de redução de risco → faixa de SIL.

SIL ALCANÇADO · projeto e verificação

5 — Documentar o SIL-alvo na SRS

Especificação de Requisitos de Segurança orienta o projeto elétrico/eletrônico.

6 — Projetar a arquitetura E/E/PE

Redundância (1oo2, 2oo3...), cobertura de diagnóstico e HFT necessários.

7 — Calcular o SIL alcançado

FMEDA de PFD/PFH a partir dos componentes reais e da arquitetura escolhida.

8 — Validar, avaliar e manter

Avaliação independente (SIL 2/3) e plano de teste periódico de prova.

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Comparativo de Níveis de Integridade

PFH (Falhas/10^9 h)	IEC 61508 (SIL)	IEC 62061 (SILCL)	ISO 13849 (PL)	ISO 26262 (ASIL)	DO 178B (DAL)	Nível de Segurança
10.000 ≤ PFH ≤ 100.000	–	–	A	–	D, E	**BAIXO**
3.000 ≤ PFH ≤ 10.000	1	1	B	–	C	
1.000 ≤ PFH ≤ 3.000			C	A	–	
100 ≤ PFH ≤ 1.000	2	2	D	B	–	
10 ≤ PFH ≤ 100	3	3	E	C	B	
1 ≤ PFH ≤ 10	4	–	–	D	–	
PFH ≤ 1	–	–	–	–	A	**ALTO**

PFH : Probability of Failure per Hour (Probabilidade de Falha por Hora).

Fonte: Adaptado de Microchip – AN6322 – Functional Safey by Decomposition – e-Fuse/Arc Faul Detection Application Example

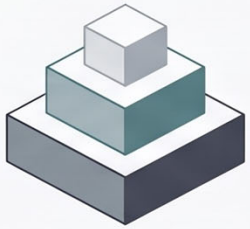
IEC 60730

MATRIZ DE CONFORMIDADE IEC 60730: CLASSES DE SEGURANÇA DE SOFTWARE

HIERARQUIA DE SEGURANÇA E RISCO

Níveis de Criticidade de Software
Define se o software é responsável por prevenir perigos imediatos ou se é não-crítico.

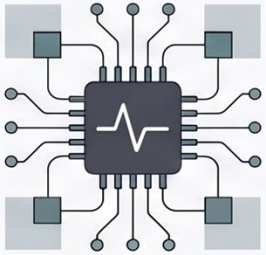
Aplicações Práticas por Classe
De controles de iluminação simples a sistemas de combustão de alto risco.



MATRIZ DE COMPARAÇÃO: REQUISITOS E APLICAÇÕES DAS CLASSES

CRITÉRIO	CLASSE A	CLASSE B	CLASSE C
Objetivo de Segurança	Funções não relacionadas à segurança.	Prevenir perigos em caso de falhas de hardware.	Prevenir perigos sem depender de outros protetores.
Nível de Risco	Baixo / Inexistente	Moderado (ex: Superaquecimento)	Alto (ex: Explosão ou Incêndio)
Exemplos de Aplicação	Eletrodomésticos gerais (ajustes de interface).	Desligamento térmico (limites de temperatura).	Controles de queimadores a gás automáticos.
Requisitos de Diagnóstico	Nenhum requisito específico de autoteste.	Testes de CPU (Reg/PC), RAM, Clock e CRC.	Diagnósticos exaustivos para falhas de alto risco.

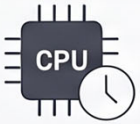
REQUISITOS TÉCNICOS DE DIAGNÓSTICO



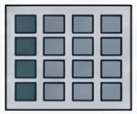
Monitoramento de Integridade do Hardware
Exigências de testes para CPU, memória e clock para garantir operação segura e contínua.

Detecção de Falhas "Stuck-at" e DC
Identificação de bits presos em registradores e falhas de acoplamento em memórias voláteis.

DETALHAMENTO DE AUTOTESTES (CLASSE B E C)



CPU e Program Counter
Verificação de bits presos e monitoramento de fluxo via Watchdog Timer em modo janela.

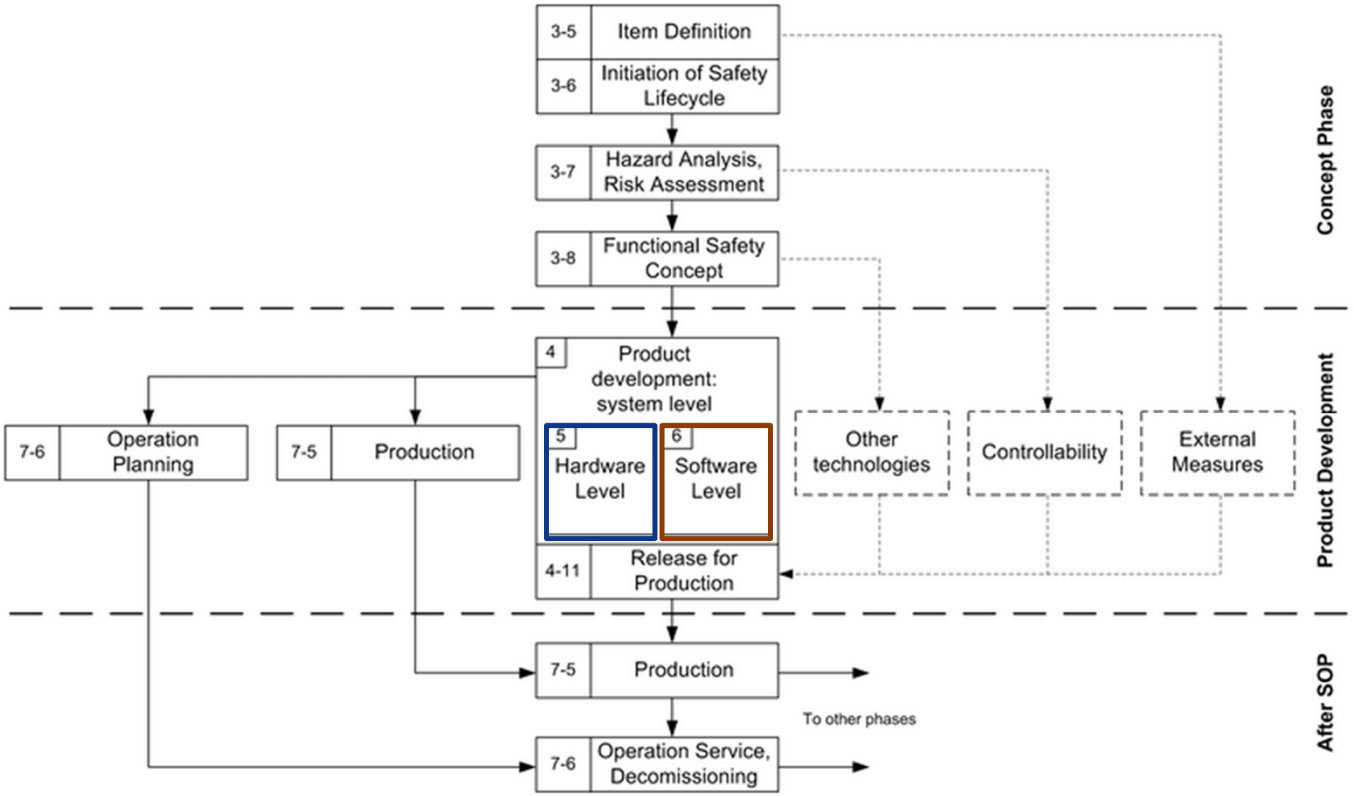


RAM e Memória Invariável
Testes de March X para SRAM e verificações de CRC para Flash/EEPROM.

Clock e Temporização
Monitoramento da frequência do sistema para detectar desvios fora da especificação técnica.

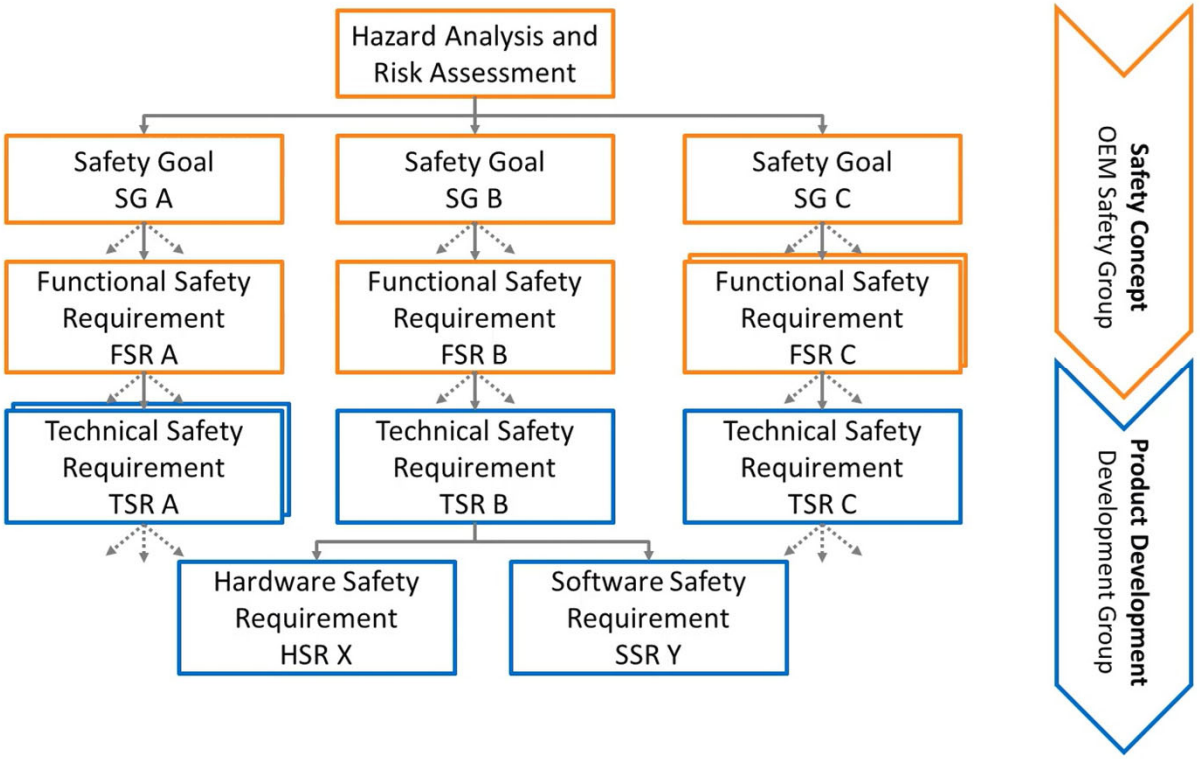
ISO 26262

Ciclo de Vida de Segurança Funcional ISO 26262



Schätz, Bernhard & Voss, Sebastian & Zverlov, Sergey. (2015). Automating Design-Space Exploration: Optimal Deployment of Automotive SW-Components in an ISO26262 Context *. 2015. 10.1145/2744769.2747912.

Projeto FuSa



Automotive Safety Integrity Level – ASIL

O ASIL é atribuído a um perigo e herdado de metas e requisitos de segurança.

Gravidade do dano
S1 – lesões leves e moderadas
S2 – lesões graves e com risco de morte
S3 – risco de morte – sobrevivência incerta

Probabilidade de exposição
E1 – probabilidade extremamente baixa
E2 – probabilidade baixa
E3 – probabilidade média
E4 – probabilidade alta

Controlabilidade pelo condutor
C1 – facilmente controlável
C2 – normalmente controlável
C3 – difícil de controlar ou incontrolável

QM é Gestão da Qualidade sem requisitos de Segurança Funcional (FuSa)

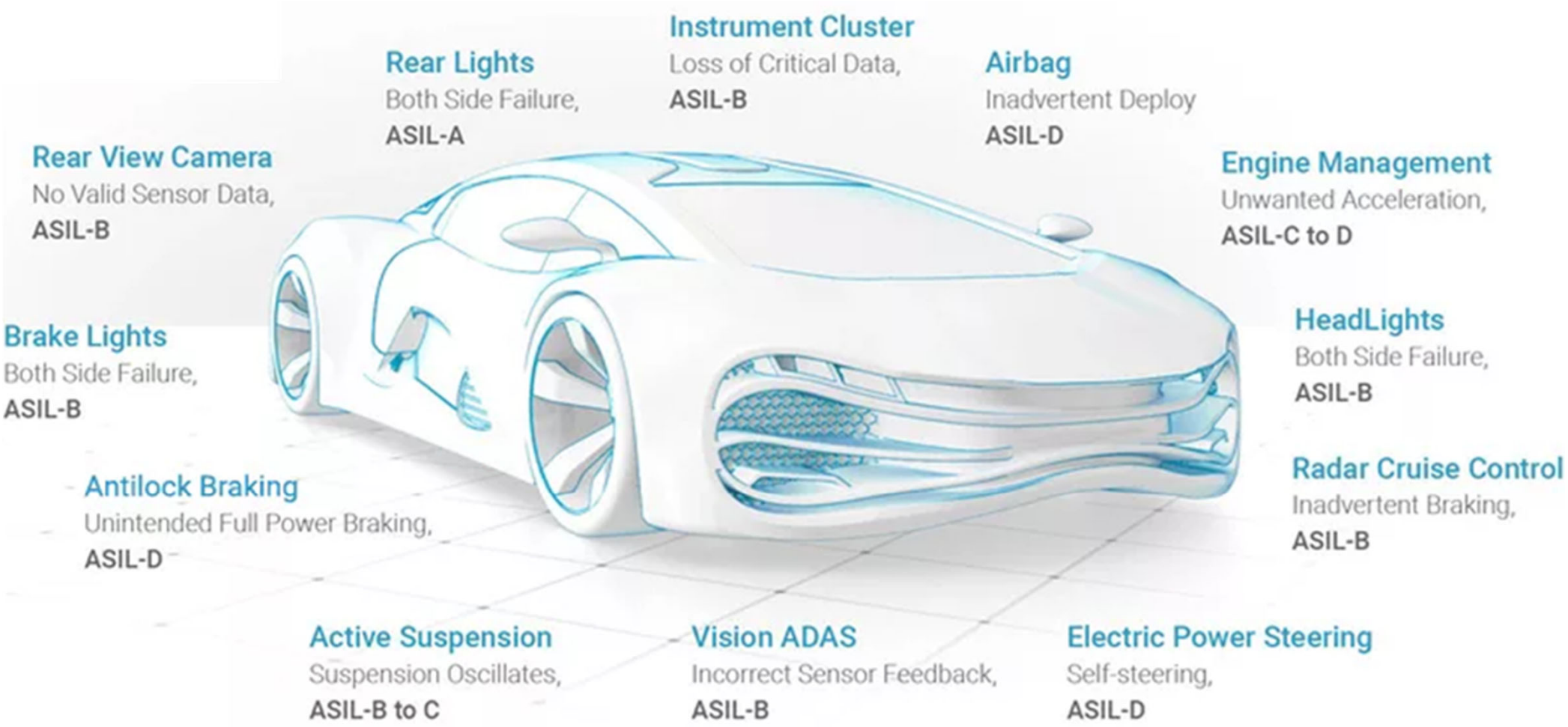
Severity	Exposure	Controllability		
		C1 (simple)	C2 (normal)	C3 (difficult)
S1 (light)	E1 (very low)	QM	QM	QM
	E2 (low)	QM	QM	QM
	E3 (medium)	QM	QM	ASIL A
	E4 (high)	QM	ASIL A	ASIL B
S2 (severe)	E1 (very low)	QM	QM	QM
	E2 (low)	QM	QM	ASIL A
	E3 (medium)	QM	ASIL A	ASIL B
	E4 (high)	ASIL A	ASIL B	ASIL C
S3 (fatal)	E1 (very low)	QM	QM	ASIL A
	E2 (low)	QM	ASIL A	ASIL B
	E3 (medium)	ASIL A	ASIL B	ASIL C
	E4 (high)	ASIL B	ASIL C	ASIL D

O ASIL não é uma propriedade de um elemento, como uma MCU.

Automotive Safety Integrity Level – ASIL

Failure merics for each ASIL level			
ASIL	Failure rate	SPFM(%)	LFM(%)
A	<1000 FIT	Not relevant	Not relevant
B	<100 FIT	90	60
C	<100 FIT	97	80
D	<10 FIT	99	90

- **FIT** significa **Failure In Time** (Falha em Tempo). 1 FIT representa exatamente 1 falha a cada 10^9 (1 bilhão) de horas de operação do componente.
- **SPFM** significa **Single-Point Fault Metric** (Métrica de Falha de Ponto Único).
- **LFM** significa **Latent Fault Metric** (Métrica de Falha Latente).



https://www.synopsys.com/glossary/what-is-asil.html

MICROCHIP

O que a Microchip oferece para suportar projetos com requisitos FuSa?

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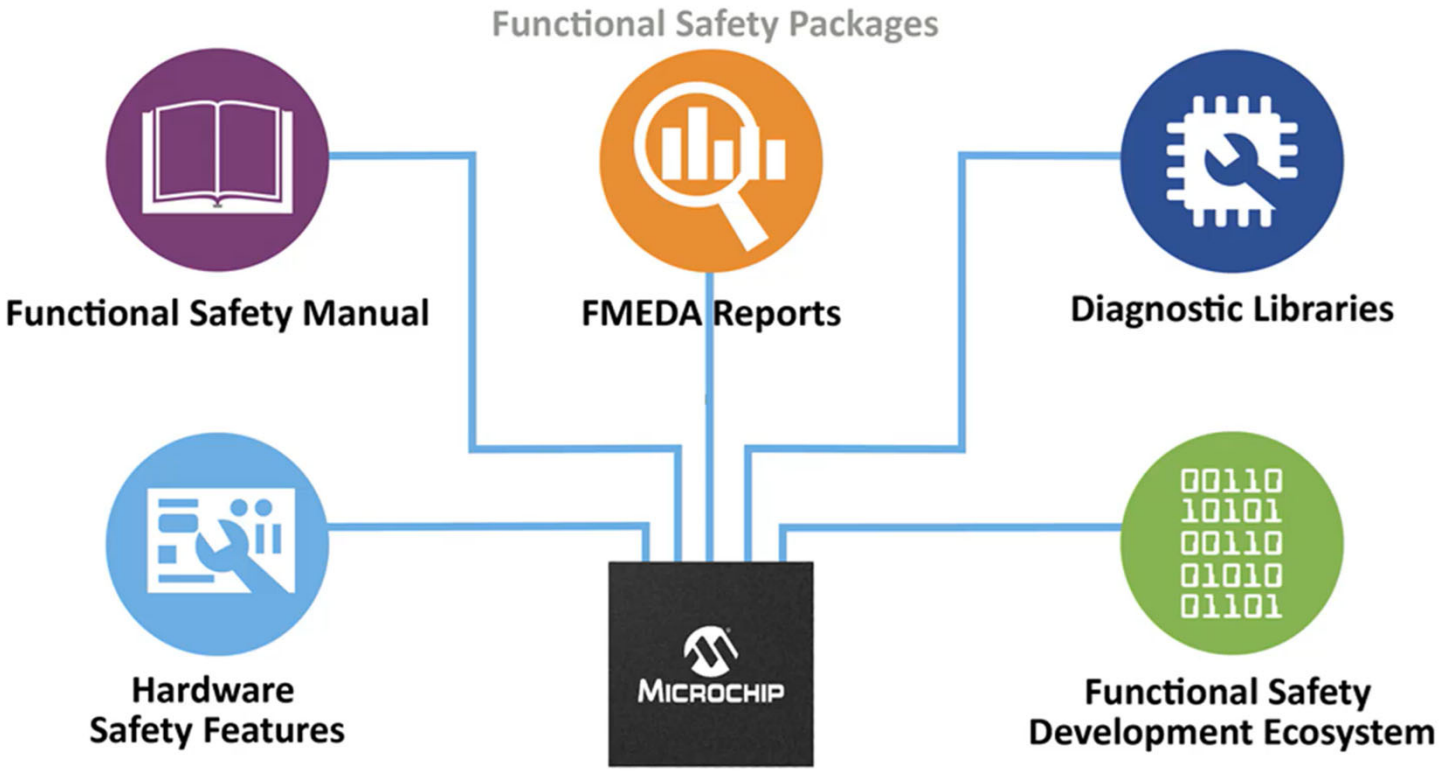
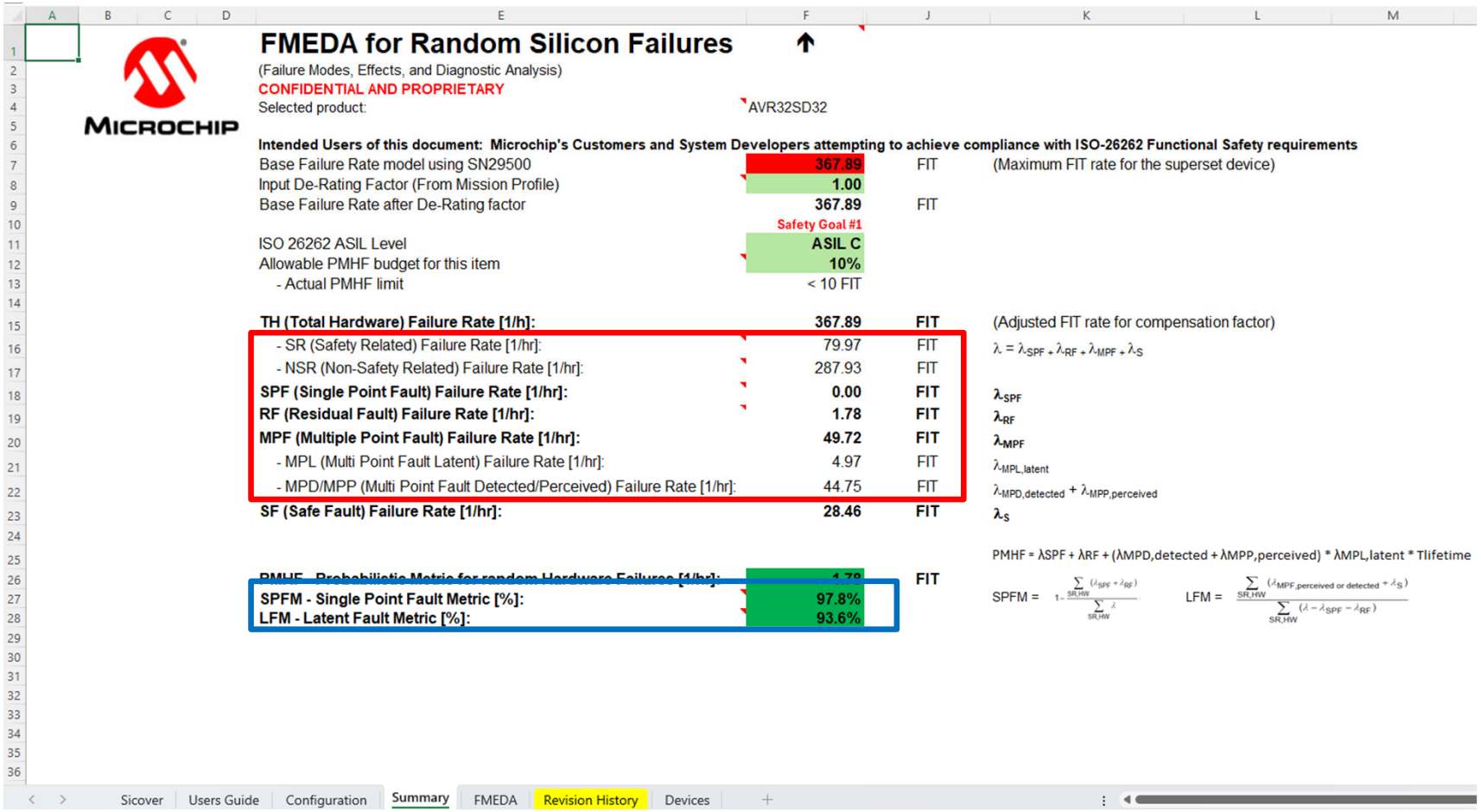


MICROCHIP

FMEDA DO DISPOSITIVO – Exemplo



FMEDA for Random Silicon Failures

(Failure Modes, Effects, and Diagnostic Analysis)

CONFIDENTIAL AND PROPRIETARY

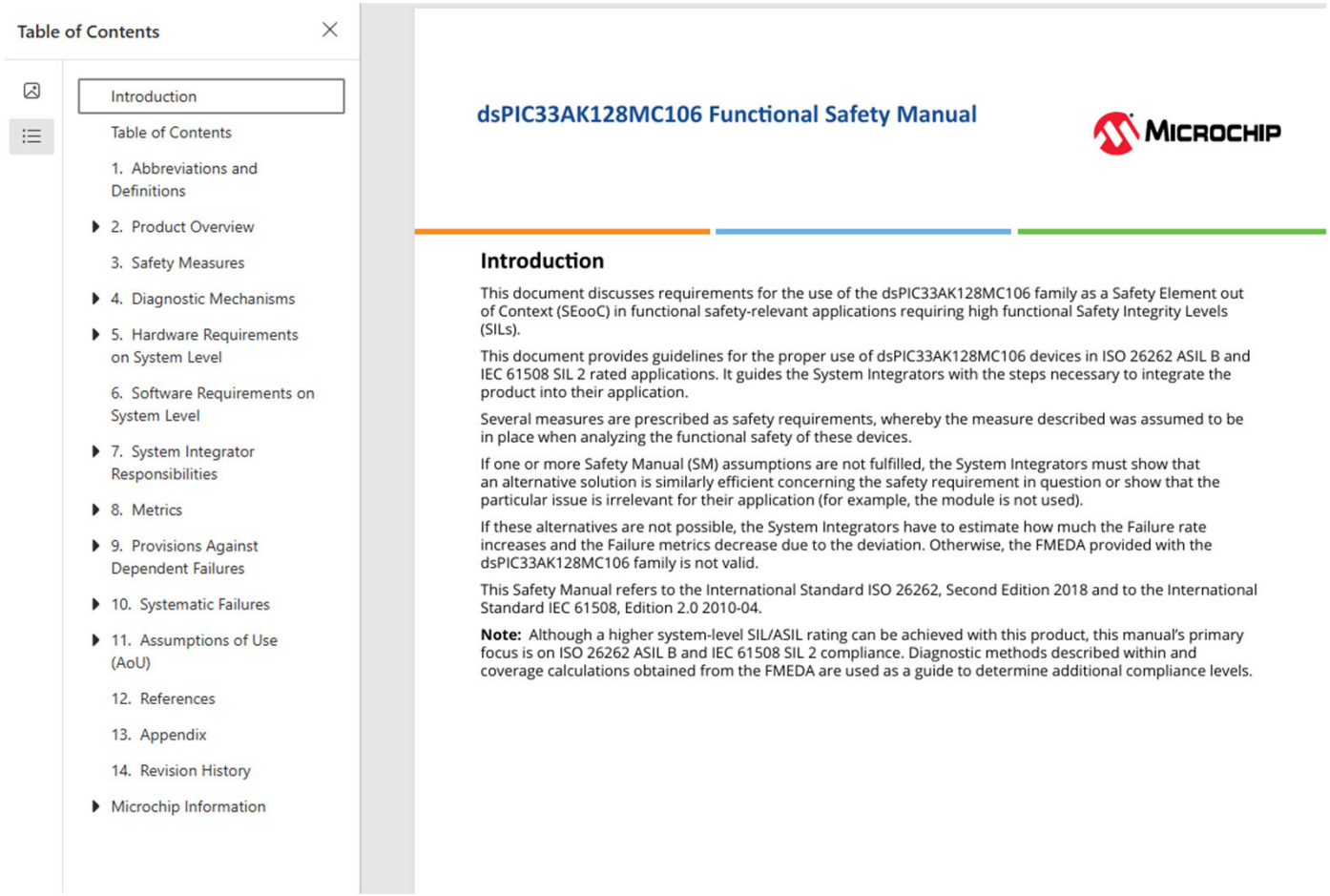
Selected product: AVR32SD32

Intended Users of this document: Microchip's Customers and System Developers attempting to achieve compliance with ISO-26262 Functional Safety requirements

Base Failure Rate model using SN29500	367.89	FIT	(Maximum FIT rate for the superset device)
Input De-Rating Factor (From Mission Profile)	1.00		
Base Failure Rate after De-Rating factor	367.89	FIT	
	Safety Goal #1		
ISO 26262 ASIL Level	ASIL C		
Allowable PMHF budget for this item	10%		
- Actual PMHF limit	< 10 FIT		
TH (Total Hardware) Failure Rate [1/h]:	**367.89**	**FIT**	(Adjusted FIT rate for compensation factor)
- SR (Safety Related) Failure Rate [1/hr]:	79.97	FIT	$\lambda = \lambda_{SPF} + \lambda_{RF} + \lambda_{MPF} + \lambda_S$
- NSR (Non-Safety Related) Failure Rate [1/hr]:	287.93	FIT	
SPF (Single Point Fault) Failure Rate [1/hr]:	**0.00**	**FIT**	λ_{SPF}
RF (Residual Fault) Failure Rate [1/hr]:	**1.78**	**FIT**	λ_{RF}
MPF (Multiple Point Fault) Failure Rate [1/hr]:	**49.72**	**FIT**	λ_{MPF}
- MPL (Multi Point Fault Latent) Failure Rate [1/hr]:	4.97	FIT	$\lambda_{MPL,latent}$
- MPD/MPP (Multi Point Fault Detected/Perceived) Failure Rate [1/hr]:	44.75	FIT	$\lambda_{MPD,detected} + \lambda_{MPP,perceived}$
SF (Safe Fault) Failure Rate [1/hr]:	**28.46**	**FIT**	λ_S
			PMHF = λSPF + λRF + (λMPD,detected + λMPP,perceived) * λMPL,latent * Tlifetime
PMHF - Probabilistic Metric for random Hardware Failures [1/hr]:	**1.78**	**FIT**	
SPFM - Single Point Fault Metric [%]:	**97.8%**		$SPFM = 1 - \frac{\sum_{SR,HW}(\lambda_{SPF} + \lambda_{RF})}{\sum_{SR,HW}\lambda}$
LFM - Latent Fault Metric [%]:	**93.6%**		$LFM = \frac{\sum_{SR,HW}(\lambda_{MPF,perceived\ or\ detected} + \lambda_S)}{\sum_{SR,HW}(\lambda - \lambda_{SPF} - \lambda_{RF})}$

Sicover | Users Guide | Configuration | Summary | FMEDA | Revision History | Devices

Manual de Segurança Funcional



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Rotinas de diagnóstico

SRAM
- SW_SRAM_REPLICATION_PRACTICE_01 (O)
- SW_SRAM_ECC_SINGLE_DOUBLE_ERROR_DETECTION_TEST_01(S,P,O)

FLASH
- SW_FLASH_ECC_SINGLE_DOUBLE_ERROR_DETECTION_TEST_01(S,P,O)
- SW_FLASH_INTEGRITY_READ_PRACTICE_01(P,O)
- SW_FLASH_WRITE_VERIFY_PRACTICE_01(O)
- SW_FLASH_MEMORY_CRC_PRACTICE_01(S,P,O)

GPIO
- SW_GPIO_PORTS_INPUT_PRACTICE_01(S,P,O)
- SW_GPIO_PORTS_OUTPUT_TEST_01(S,P,O)
- SW_GPIO_ACTIVITY_CHECK_01(O)
- SW_GPIO_PORTS_INTERRUPT_GENERATION_TEST_01(S,P,O)
- SW_GPIO_PPS_OUTPUT_CONNECTION_TEST_01 (S,P,O)
- SW_IO_MONITOR_TEST_01 (S,P,O)

INTS
- SW_INTERRUPT_SERVICING_TEST_01 (S,P,O)
- SW_EXTERNAL_INTERRUPT_TEST_01 (S,P,O)
- SW_INTERRUPT_FREQUENCY_CHECK_01(O)
- SW_HARD_TRAP_TEST_01(S,P,O)
- SW_ISR_CLEARED_CHECK_01(O)

TIMER
- SW_TIMER_FUNCTIONAL_TEST_02(S,P,O)
- SW_TIMER_LINEARITY_TEST_01(P)

CPU
- SW_CPU_REGISTER_RESET_STATE_TEST_01(S)
- SW_CPU_CONTROL_REGISTER_TEST_01(S,P,O)
- SW_CPU_SELF_TEST_01(P,O)

UART
- SW_UART_AUTOBAUD_TEST_01(S,P,O)
- SW_UART_FLOW_CONTROL_TEST_01(S,P,O)
- SW_UART_LOOPBACK_SELF_TEST_01 (S,P,O)
- SW_UART_RX_FUNCTIONAL_TEST_01(S,P,O)
- SW_UART_STATUS_MONITOR_TEST_01(S,P,O)
- SW_UART_TX_FUNCTIONAL_CHECK_01(O)
- SW_LIN_CHECKSUM_TEST_01(S,P,O)
- SW_LIN_RX_FRAME_TEST_01(S,P,O)
- SW_LIN_TX_FRAME_TEST_01(S,P,O)

ADC
- SW_ADC_BOUNDARY_MONITOR_TEST_01(S,P,O)
- SW_ADC_LINEARITY_MONOTONICITY_TEST_01(S,P,O)
- SW_ADC_STARTUP_TEST_01 (S,P,O)

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Pacotes de Segurança Funcional

ISO 26262 - Automotive Functional Safety Packages Overview
IEC 61508 - Industrial Functional Safety Packages Overview

Packages	Functional Safety Sample Package	Functional Safety Basic Package (BPACK)	Functional Safety Standard Package (SPACK)
Sales channel	(Free)	Microchip Direct and Distribution	
Description	Sample FMEDA Sample Safety Manual IEC 60730 library	FMEDA Safety Manual	FMEDA Safety Manual Selected Diagnostic library(1)
Products covered	Generic	One device family	One device family
Validity	N/A	Updates include for one year	
Price (8-bit MCUs)	**Free**	**$999**(2)(3)	**$1999**(2)(3)
Price (32-bit MCUs)	**Free**	**$999**(2)(3)	**$4999**(2)(3)
Price (dsPIC)		**$3000**	**$10000**
Distribution of products	Microchip Web	Download via Microchip Direct	Download via Microchip Direct
Terms and Conditions	Registration	Registration and CLA	

Notes (1) Highly recommended to use XC Functional Safety Pro compiler with the diagnostic library
For **8 bit MCUs**, does not include peripheral diagnostics / **32 bit MCUs**, core diagnostics include CPU self test library and selected peripheral modules.
Price and Selected diagnostic library detail is available in mD
(2) Above price is negotiable via BDM/CMT.
(3) mD download login validity time is 18 months. BDM/CEM can reach out, or customer can contact us to extend.

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Pacotes de Segurança Funcional

ZERTIFIKAT ◆ CERTIFICATE ◆ 認證證書 ◆ СЕРТИФИКАТ ◆ CERTIFICADO ◆ CERTIFICAT

CERTIFICATE
No. Z10 106936 0001 Rev. 02

Holder of Certificate: Microchip Technology Inc.
2355 W. Chandler Boulevard
Chandler AZ 85224
USA

Certification Mark:

Product: Software Tool for Safety Related Development

Model(s): MPLAB® XC8 C Compiler
MPLAB® XC-DSC C Compiler
MPLAB® XC32 C/C++ Compiler

Parameters: The compiler is qualified to be used in safety-related software development according to ISO 26262 for any ASIL, IEC 61508 for any SIL, EN 50128 for any SIL, and IEC 60730-1. It is suitably validated for use in safety-related development according to IEC 62304.
The report MC94582C is a mandatory part of this certificate.

Tested according to: ISO 26262-8:2018
IEC 61508-3:2010
IEC 62304:2006
IEC 62304:2006/AMD1:2015
EN 50128:2011/A1:2020
IEC 60730-1:2022

The product was tested on a voluntary basis and complies with the essential requirements. The certification mark shown above can be affixed on the product. It is not permitted to alter the certification mark in any way. In addition the certification holder must not transfer the certificate to third parties. This certificate is valid until the listed date, unless it is cancelled earlier. All applicable requirements of the Testing, Certification, Validation and Verification Regulations of TÜV SÜD Group have to be complied. For details see: www.tuvsud.com/ps-cert

Test report no.: MC94582C
Valid until: 2029-05-28
Date, 2024-05-31

(Peter Weiß)

Page 1 of 1
TÜV SÜD Product Service GmbH • Certification Body • Ridlerstraße 65 • 80339 Munich • Germany

- **Relatórios de Classificação e Análise**
  - Gen 4/5 HW Tools
  - MPLAB Analysis Tool Suite **(Free)**
  - MPLAB X IDE **(Free)**
  - MPLAB XC32/XC-DSC/XC8 **(Free)**
  - LIBERO (FPGA E SOC) (Algumas versões FREE)
- **Relatórios de qualificação de compiladores**
- **Manual de segurança funcional do compilador**
- **Relatório da TÜV sobre o certificado**
  - Escopo da certificação

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High-performance standard and specialized mixed-signal Microcontroller, Digital Signal Controller and Microprocessor solutions

Mixed-signal, Analog, Interface and Security solutions

Clock and timing solutions

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FPGA solutions

Non-volatile EEPROM and Flash memory solutions

Flash IP solutions

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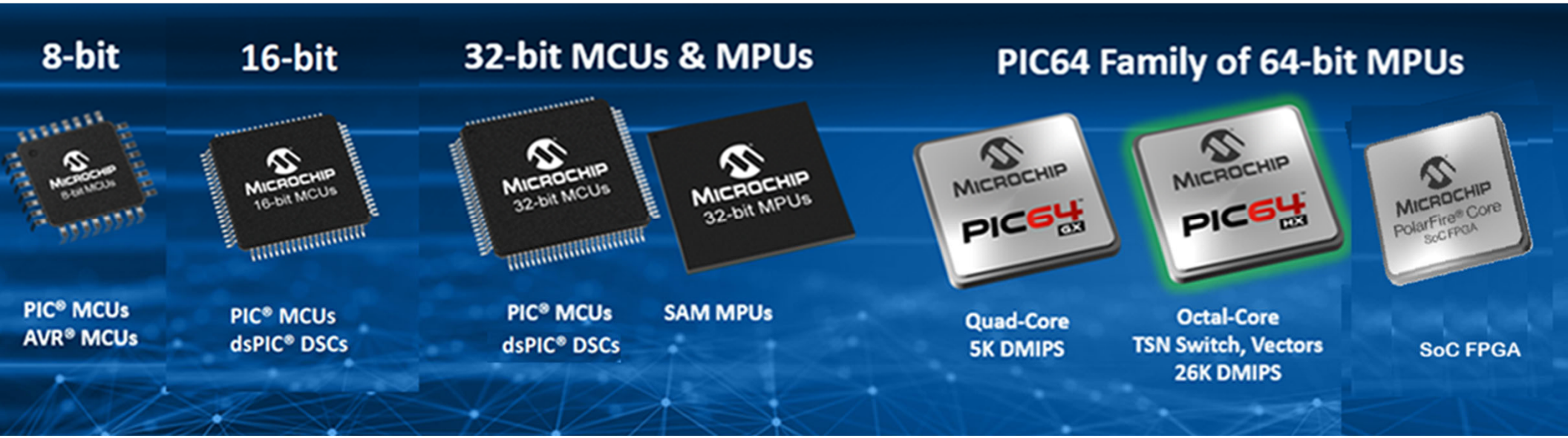
PORTFOLIO DE CPUs



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MCUs 8 bits - AVR

https://www.microchip.com/en-us/products/microcontrollers/8-bit-mcus/avr-mcus

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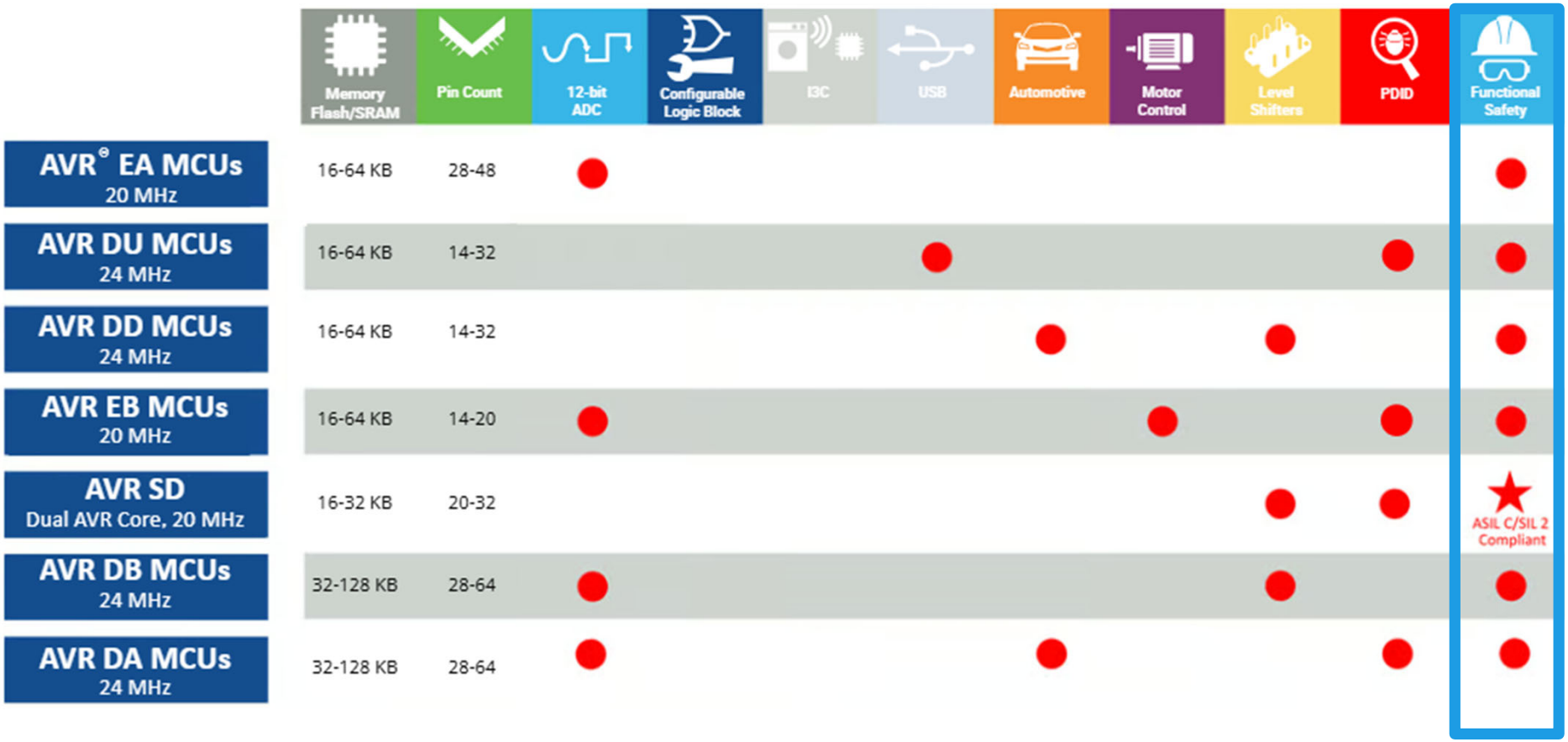
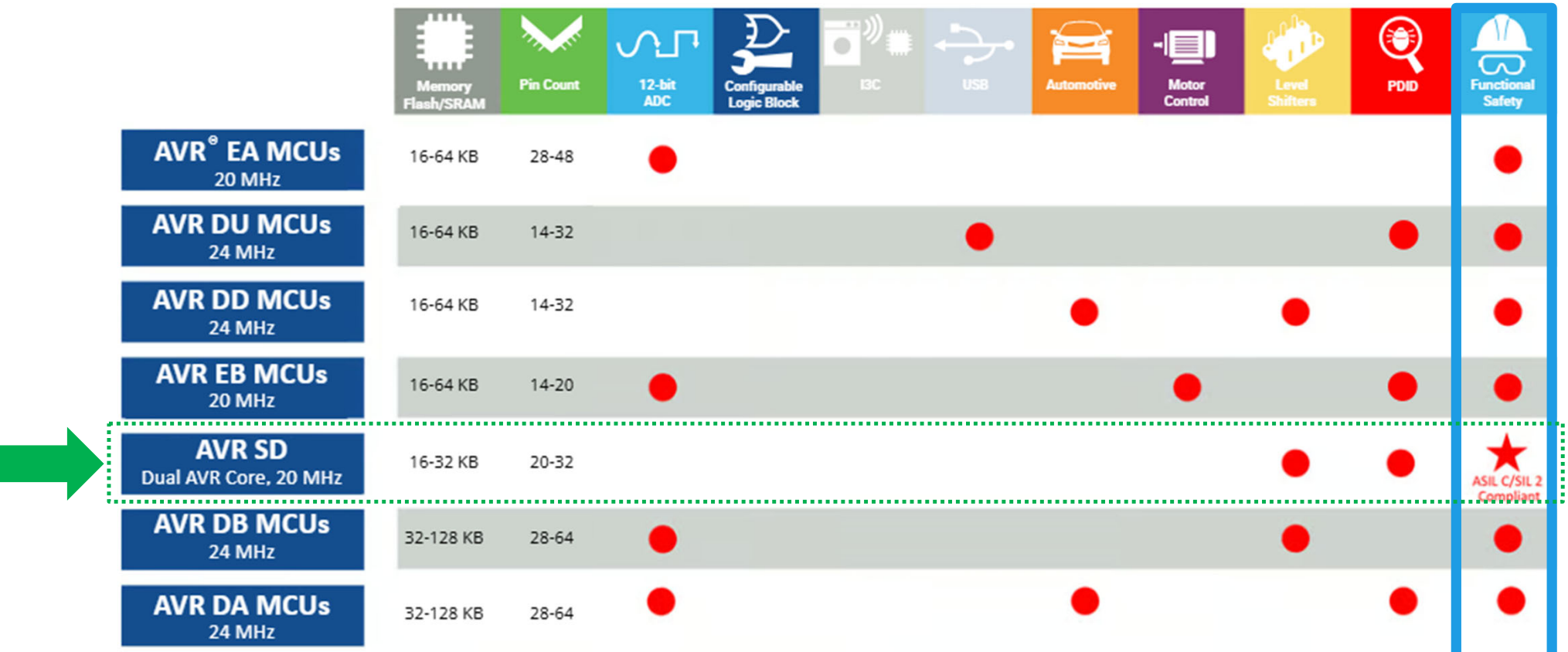


MCUs 8 bits - AVR

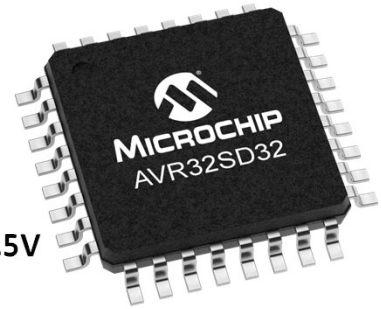
https://www.microchip.com/en-us/products/microcontrollers/8-bit-mcus/avr-mcus



AVR® SD MCU – Família de MCUs com Segurança Funcional Aprimorada

Projetado em conformidade com a norma de segurança funcional ISO 26262 para aplicações ASIL C/SIL 2

- **Dual-core lockstep CPU**
- **20 MHz CPU clock speed**
- **Flash/SRAM/EEPROM with ECC:**
- **512B User row**
- **256B Key storage**
- **Faixa de tensão de alimentação 2.7V – 5.5V**
- **Industrial and extended temp range**
  - -40°C to 85°C and -40°C to 125°C
- **Características especiais**
  - Multi-Voltage IO (MVIO)
  - Event System (EVSYS)
  - Configurable Custom Logic (CCL)
  - Programming and Debug Interface Disable (PDID)

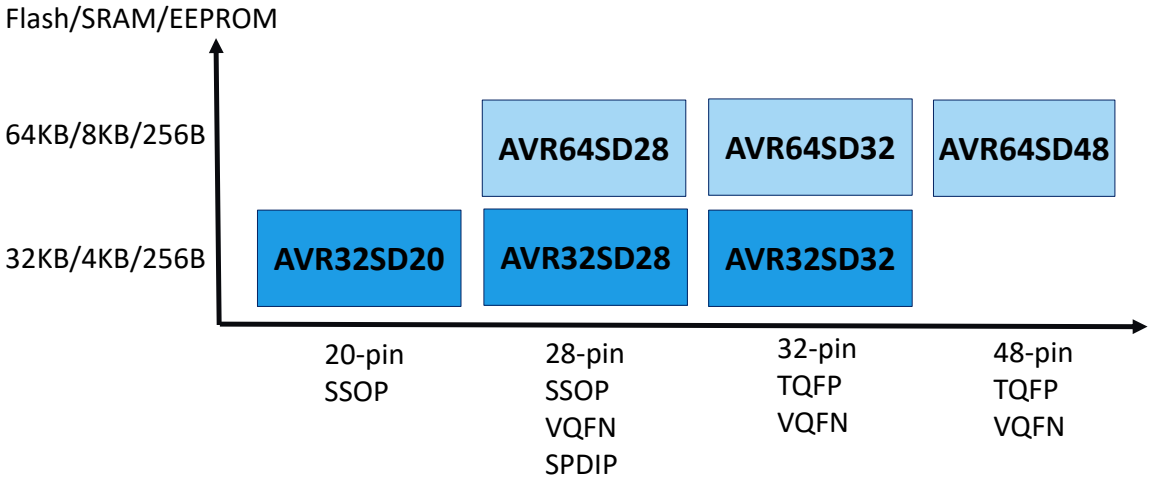


- **Circuitos Analógicos**
  - 2x 10-bit single-ended ADCs
  - 1x 10-bit DAC
  - 3x analog comparators
  - 2x Zero-Cross Detectors (ZCD)
- **Watchdogs**
  - Asynchronous Window Watchdog (WDT)
  - Synchronous Window Watchdog (SWDT)

Automotive-grade ordering codes (VAO suffix) are set up on request and not listed in *Available Product Numbers*.

AVR® SD MCU – Família de MCUs com Segurança Funcional Aprimorada

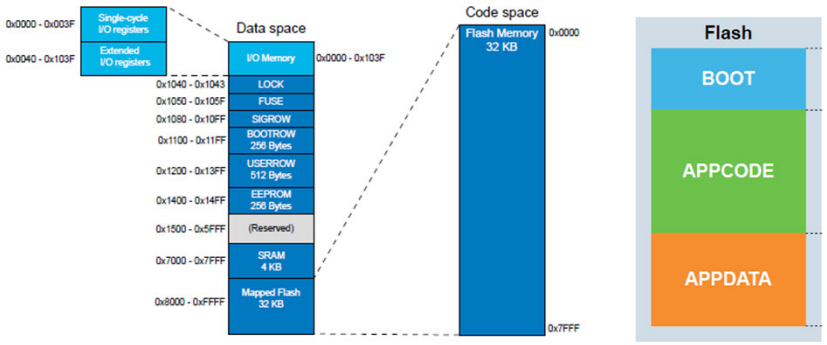
Projetado em conformidade com a norma de segurança funcional ISO 26262 para aplicações ASIL C/SIL 2

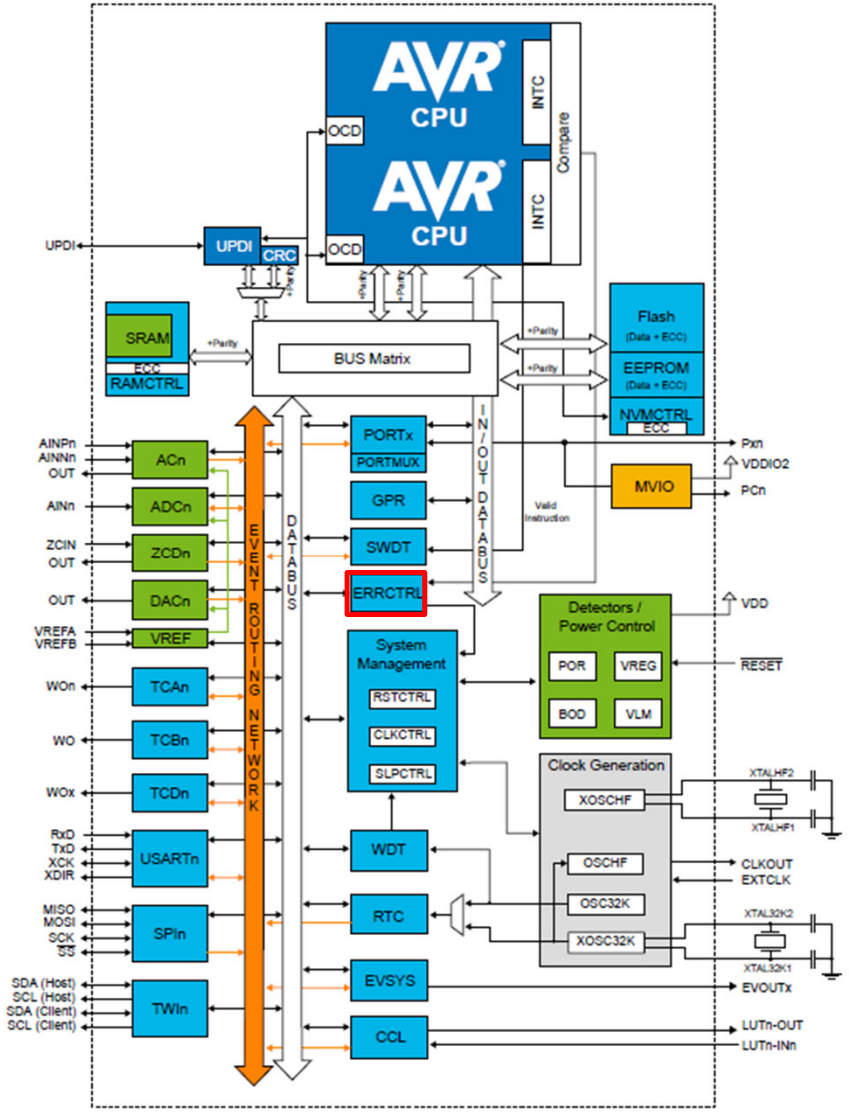


Automotive-grade ordering codes (VAO suffix) are set up on request and not listed in *Available Product Numbers*.

AVR® SD MCU

Mapa da Memória





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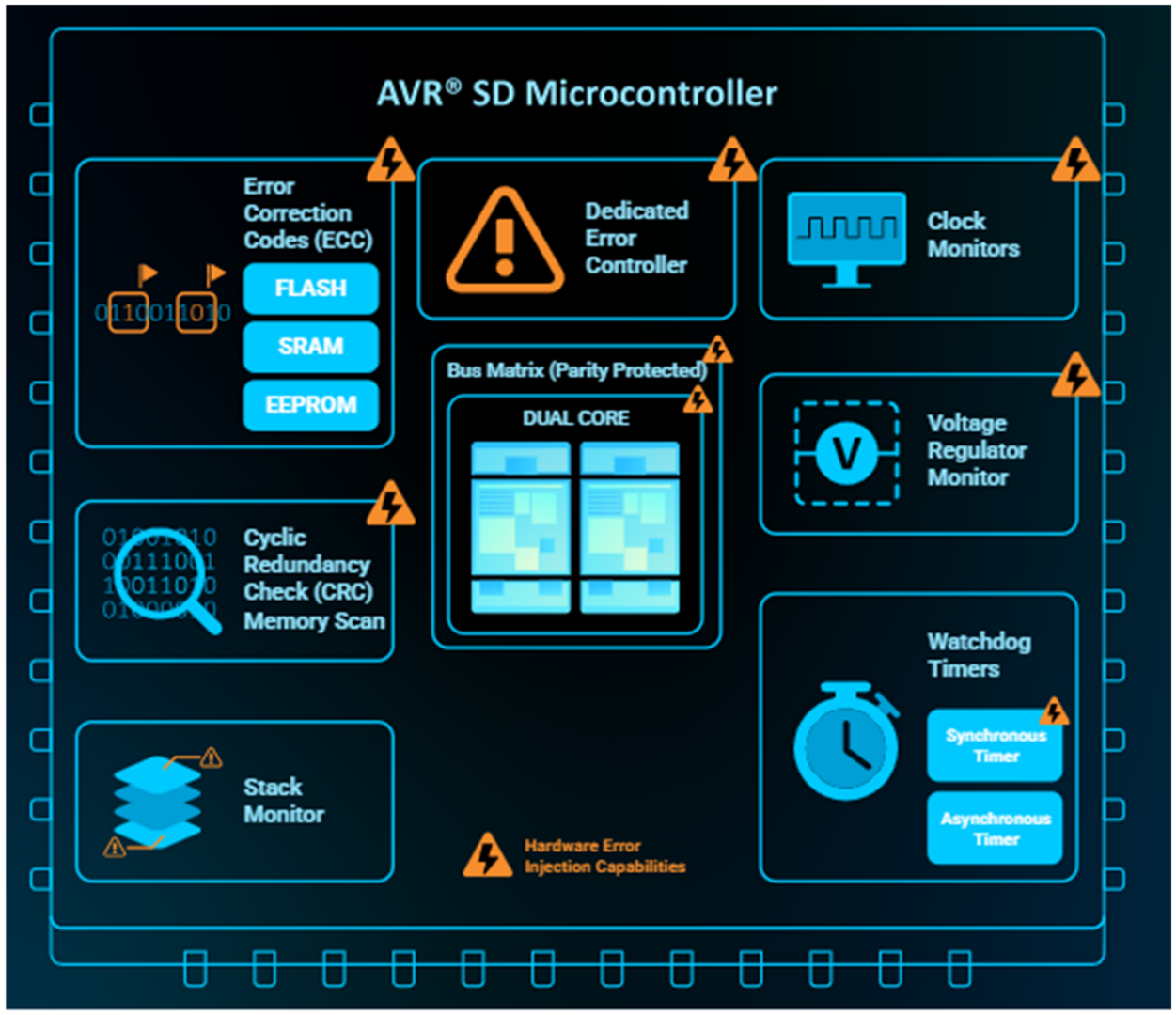
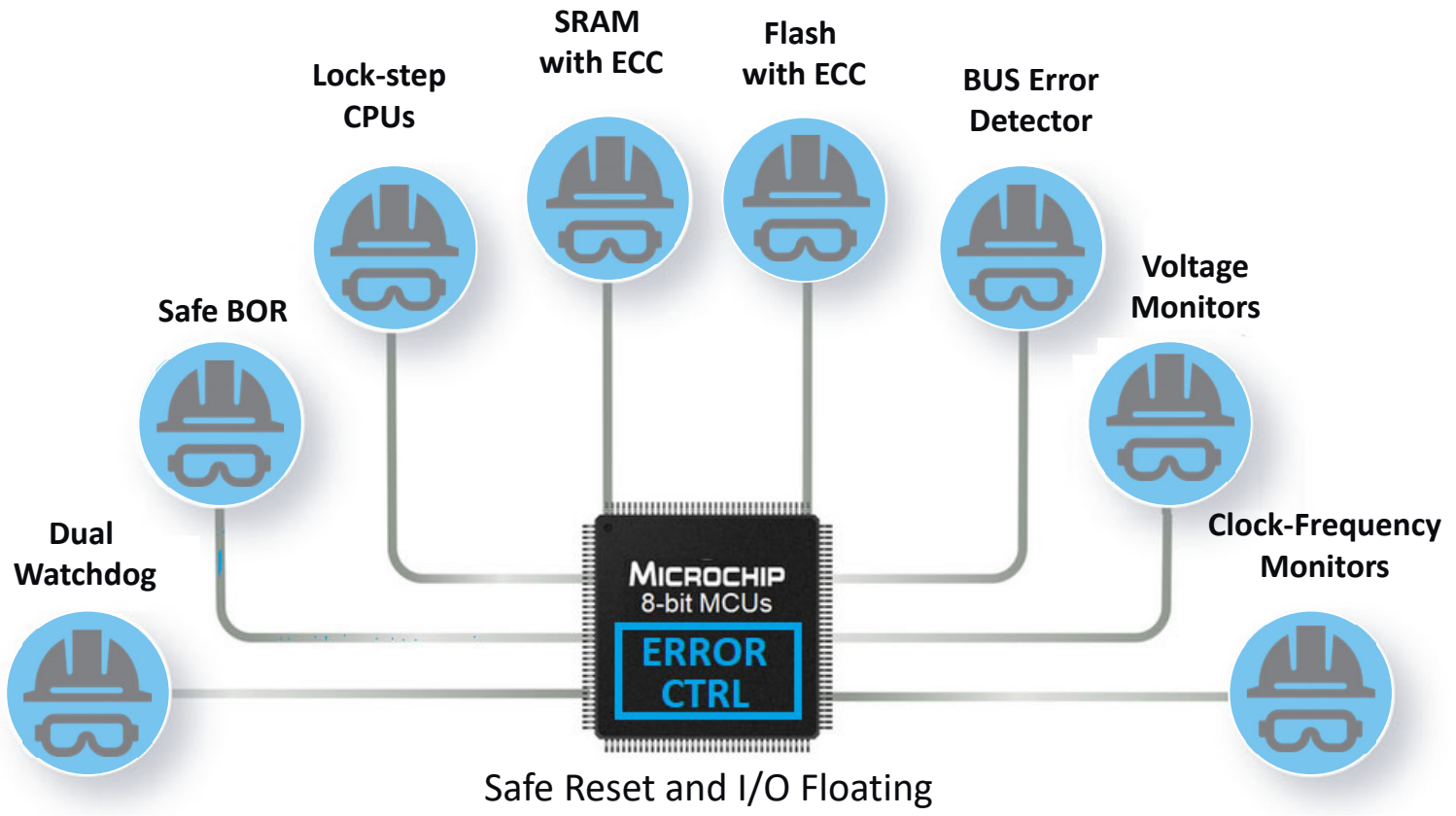


Core Independent Safety (CIS)

Enables Real-Time Safety and Reduce CPU Load



AVR32SD32 (EV75S16A) Curiosity Nano Evaluation Kit

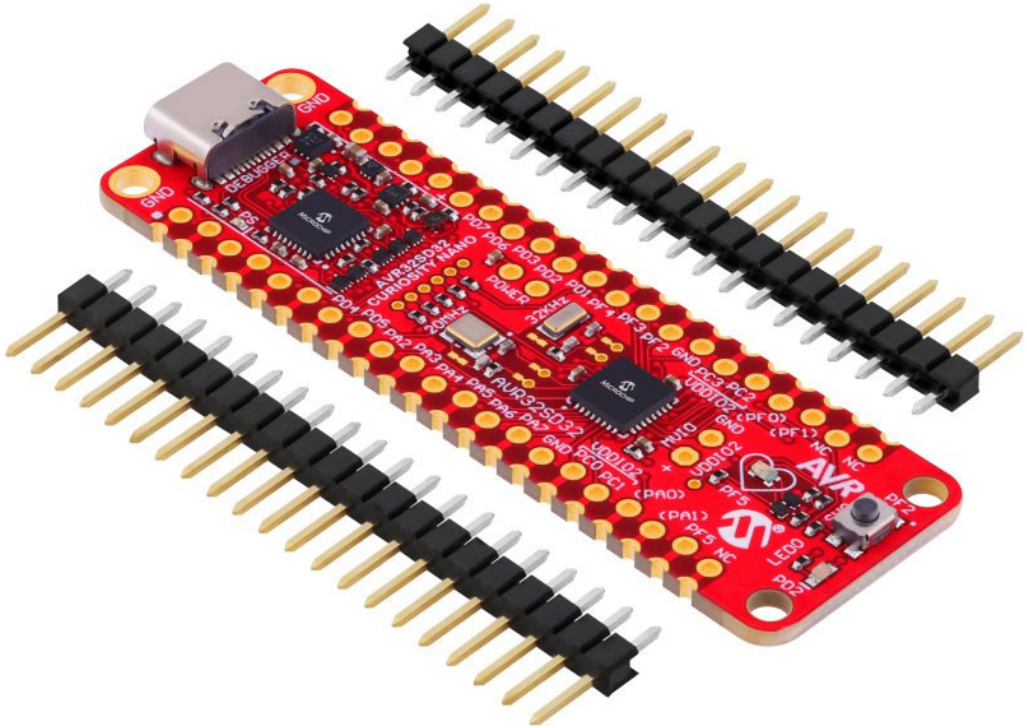


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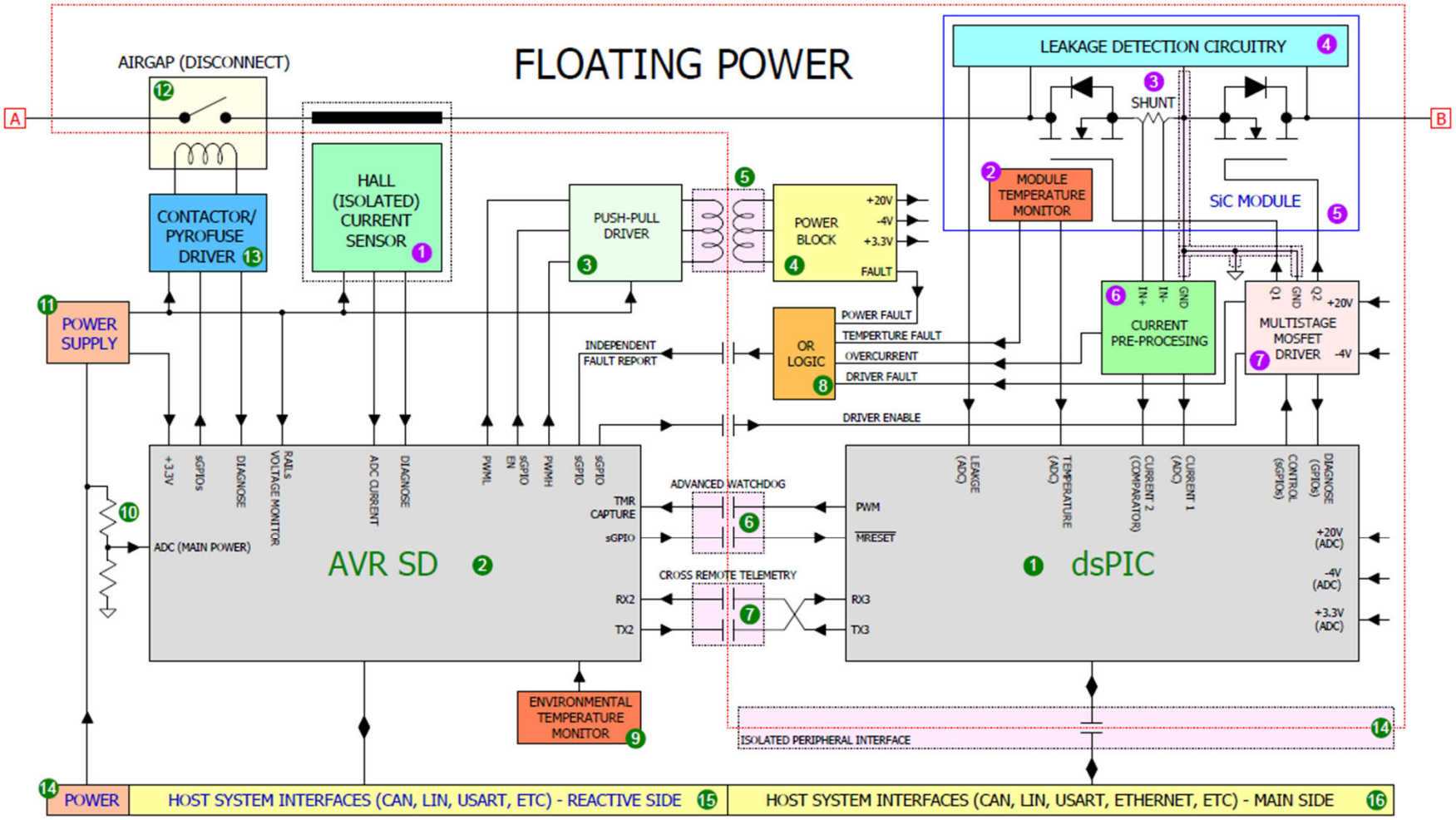
Figure 3-1. High SIL e-Fuse Practical Architecture



Fonte: Microchip – AN6322 – Functional Safey by Decomposition – e-Fuse/Arc Faul Detection Application Example

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